Design of ESD protections for ECG applications

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***Abstract*—This paper presents the design of Electrostatic Discharge (ESD) protections for a remote Electroencephalograph (ECG). Design and layout guidelines are analyzed to improve the ESD robustness of a Grounded-Gate NMOS (GGNMOS) cell based on a single well CMOS-only process. Experimental validation is done by means of a Time Domain Reflectometry (TDR) technique known as Transmission Line Pulse (TLP) testing. The silicon implementation of the proposed design passes ±3700V in the Human-Body Model (HBM).**

Keywords*— *Electroencephalography (ECG), Electrostatic discharge (ESD), Human-Body Model (HBM), Transmission Line Pulse (TLP), Time Domain Reflectometry (TDR)

I. Introduction

The Electrostatic Discharge (ESD) robustness of electronic systems is of utmost importance in the design of any kind of electronic systems. This is particularly true for biomedical systems such as Electrocardiographs (ECG), Electroencephalograms (EEG), Oximeters, implantable devices and every single device where the life of a patient is at risk [1], [2], [3], [4] and [5]. Since electrical safety regulations do not allow grounding the patients (to drain out the electrostatic charges that may get accumulated on their skin), preventive measures to avoid these charges from damaging the electronic circuitry shall be addressed. In this regard, the Human-Body Model (HBM) standard considers the ESD strikes of human beings as double exponential waves whose rise time is in the order of 1-10ns and its fall time in the range of 100-200ns. These characteristics are very well mimicked by ESD testers, whose inner cores are nothing more than RC networks where the capacitance determines the energy of the discharge and the resistance, the decay.

Few of the educationally available Multi-Project Wafer (MPW) platforms provide basic libraries to deal with ESD events, while most lack information about it. This is the case despite the huge importance of this area in terms of safety and reliability. Moreover, limited works can be found on the bibliography concerning the low-level design of ESD structures. Consequently, this work proposes to tackle such shortage.

In [6], a cascade of 3 Grounded-Gate NMOS (GGNMOS) structures is presented as the protection mechanism for ESD hazards, with some additional RC filtering. However, neither design, layout guidelines nor measurements are presented. Moreover, the input impedance of this approach is being compromised by the filters and it won't allow to apply a chopper-stabilized topology as the ones presented in [7], [8] and [9] which will be the targeted application of this work.

In [10], a Silicon-Controlled Rectifier (SCR) on a 0.18µm CMOS process is presented with measurements that validate the performance. However, neither design nor layout guidelines are presented.

One of the main challenges in ESD design is the validation of the structures. Not only because ESD testers are rather expensive but also because the testing procedure with such equipment is self-contained. This means that ESD testers do not provide more information than a Pass / Do not pass result, making the design and debugging process quite challenging. In order to overcome with this limitation, a Time Domain Reflectometry (TDR) technique called Transmission Line Pulse (TLP) testing was used. The benefits of this approach rely not only on a cost perspective but also on the fact that it is an inherently more insightful approach that gives a better understanding of how the structures work and how do they dynamically behave against the ESD event [11]. Fig. 1 shows a theoretical comparison of both waveforms for a given amount of electrical charge.

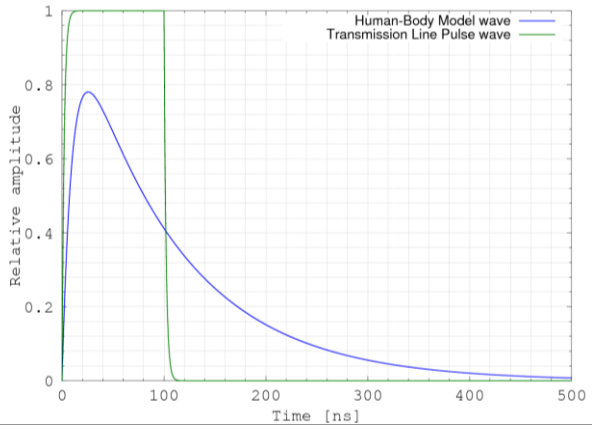

Fig. 1. Double exponential HBM wave and TLP wave.

This paper is organized as follows: Section II describes the design procedure of the ESD protections with some guidelines in terms of layout. Section III presents the TLP technique and its correlation with the HBM standard. Afterwards, the experimental results are presented in Section IV and finally, in Section V the conclusions of this paper are drawn.

II. Design

ESD is a particular case of a charge-driven event, where their movement leads to high current densities and subsequently high voltages, which result in high electric fields. Consequently, the failure modes can be either from a thermal or an electric source. In the former, Joule effect heats up the structures, while on the latter the high electric field causes charge injection or dielectric breakdown. These failures are highly dependent on the manufacturing technology, for example processes with insulated substrate such as Silicon On Insulator (SOI) and Silicon On Sapphire (SOS) have a larger thermal mass that prevents the heat from being removed as effectively as in a LOCal Oxidation of Silicon (LOCOS) process, where the energy of the ESD strike can be absorbed much more conveniently since there is no insulator acting as an electrical (and thermal) barrier [12]. On the other hand, in LOCOS processes, the interface between thick and thin oxides are usually a weak point from an electric field perspective and although this can be improved with Lightly Doped Drain (LDD) implants, it comes with larger power dissipation as it will be described afterwards.

The goal of every ESD protection is as simple as to clamp the voltage to a safe level and to provide a safe path for the high current while withstanding the energy delivered by the external source. Note that these protections are meant for handling energy events rather than power events. In fact, since the on-resistance of ESD protections is more than 2 orders of magnitude below the HBM network resistance, the ESD event can be thought as a finite-energy current source.

There are out-die and in-die protections, in the case of the former, these protections include Transient Voltage Suppressors (TVS), Gas Discharge Tubes (GDT), Metal-Oxide Varistor (MOV) or even the discrete version of in-die protections. However, the main drawback of all these devices is that they do not protect the DUT until they are properly interconnected. It leaves the front-end circuitry vulnerable during the product assembly which, in general, is one of the most critical stages in terms of ESD hazards. The most common approaches among in-die protections are simple diodes (including Zeners or even mere rectifiers), Grounded-Gate-NMOS (GGNMOS) and Silicon Controlled Rectifiers (SCR). In the case of the last two, the main drawback is the risk of having false triggering, which can cause device destruction if it happens during nominal operation.

In this work, GGNMOS structures [12], [13], [14] will be used as in [6] and [10]. In these devices, the lateral parasitic NPN buried within an NMOS is used to handle the ESD current. A schematic view of the device is shown on Fig. 2.

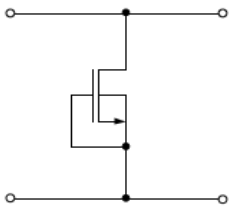

Fig. 2. Schematic of a GGNMOS protection.

With the gate grounded, the drain voltage can raise until the drain-body junction enters in avalanche breakdown (V_{t1}, I_{t1}), which should be lower than the gate oxide breakdown. At this point, current develops a voltage drop to forward bias the body-source junction injecting more electrons into the base region. After this, an snapback ocurrs and the drain voltage drops significantly as a result of the enhanced conductance of the NPN path (V_h, I_h). These values are known as holding or sustaining because going below them will turn off the bipolar. Therefore, in the design of GGNMOS structures, it is crucial that the power supply voltage (V_{dd}) and the supply current (I_{dd}) are below V_h and I_h respectively as shown on Fig. 3. Otherwise, several GGNMOS can be stacked to meet the voltage requirement.

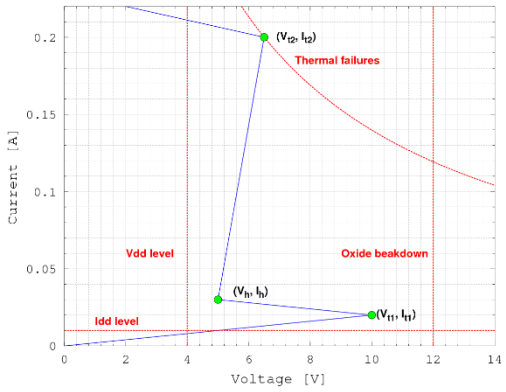

Fig. 3. GGNMOS typical I-V curve and its SOA.

On the other hand, the second or thermal breakdown point (V_{t2}) is also known as the limit of the Safety Operating Area (SOA), because stressing the device beyond it will cause a physical non-reversible change on its inner structure. Moreover, this point shall be larger than V_{t1} when multiple structures are parallelized, otherwise the branches could get destroyed one by one before the others even turn on.

Several technology parameters have to be taken into account when designing these kind of structures. For example, the thickness of the wafer (in single-well processes) or the epitaxial layer will affect the performance not only from a heat flow perspective, where the SOI and LOCOS processes are the extreme cases, but also from an electrical perspective. Because the amount of current required to trigger the parasitic NPN (at V_{t1}) will be inversely proportional to the intrinsic resistance of the well, which is defined by its physical dimensions and doping profile.

In adittion to that, LDD implants have been widely used by the industry to improve hot carrier performance since it reduces the electric field at the oxide surface preventing carriers to get stuck on it and shifting the transistor threshold as a consequence. However, the lower doping of these regions comes with a larger resistance in the channel that produces a higher V_h and more heat dissipation for a given amount of current.

On the other hand, non-uniform current densities across the multiple fingers of a GGNMOS structure is not suggested. In this scenario, an extended drain geometry as the one presented

on Fig. 4 is required to ballast the current densities. The increased resistance of this extended N+ regions guarantees a uniform current distribution among parallel GGNMOS [13]. However, low-resistance silicide can still lead to non-uniform current distribution. Therefore a blocking layer over the drain extension region is mandatory in order to force the current to flow through the n-well diffusion instead of over the silicide. This avoids not only current crowding but also current filamentation [13]. The main drawback of this approach is the obvious need of an extra mask. However, in [15] some layout techniques to avoid it are discussed for Fully-Silicided processes.

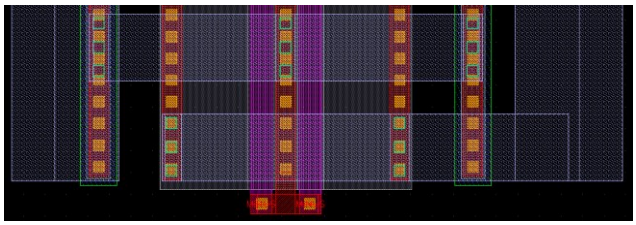

Fig. 4. Layout view of two fingers of a GGNMOS structure.

Fig. 5 shows the substrate resistance of GGNMOS structures. In the case of parallel structures, special attention should be paid to guarantee the minimum body-source resistance from one finger to the subsequent, as well as systematic increases from one structure to the next one. In terms of substrate contacts, since they provide an undesired current path for the body current, it is recommended to exclusively have them in the structure surroundings.

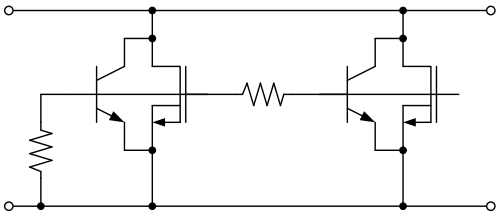

Fig. 5. Parasitic devices of the GGNMOS cells.

The protections must be placed as close as possible to the bond pads. Therefore, a GGNMOS clamp (as the one shown in Fig. 2) was implemented for every pin. The structures have been sized with a W/L=50µm/1µm to provide a compact layout in combination with the pads as shown in Fig. 6.

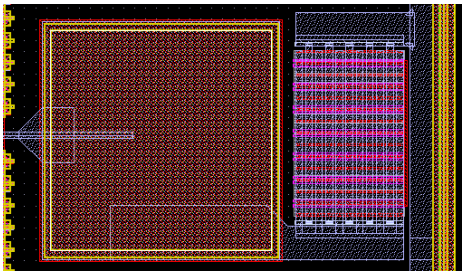

Fig. 6. Layout view of a ESD cells.

III. Characterization Bench

The Transmission Line Pulse (TLP) testing approach is a well-known technique for studying ESD protections [11]. The concept behind this Time Domain Reflectometry (TDR) technique is that the discharge pulse mimics, in terms of energy, an HBM pulse. The following picture shows the standard setup of a constant impedance TLP bench [16], where the most critical component is the fast mercury (Hg) relay that needs to guarantee a debounced contact in order to effectively deliver the ESD strike to the load. The relation between the TLP rating and the HBM equivalent rating is a factor of 1500Ω [11].

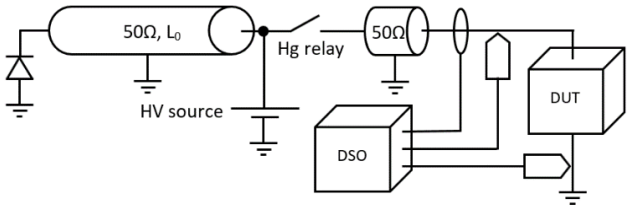

Fig. 7. Constant impedance (50Ω) TLP bench.

Pulse width turns out to be the time it takes to discharge the pre-charged transmission line of length L_0 by a travelling wave of propagation velocity v calculated in (1)

$$v \cong \frac{c_0}{\sqrt{\varepsilon_r}} \quad (1)$$

Where c_0 is the speed of light in vacuum and ε_r is the relative dielectric constant of the transmission line insulator, which for an RG-316 cable is 2.25. Therefore, for a 100ns pulse (as required to meet the HBM model [11]), 10m of cable are needed.

Several works have proved a miscorrelation between HBM and TLP results when the triggering mechanism of the protections is susceptible to the high dv/dt content of the ESD pulse [11]. To test a worst-case scenario, this works uses a rise time of 1ns and a pulse width of 100ns.

IV. Experimental Results

The GGNMOS structures have been implemented on a 0.5µm CMOS-only process by a Multi-project Wafer (MPW) Fabrication Service provided by MOSIS. Fig. 8 provides a microphotograph of the GGNMOS protection.

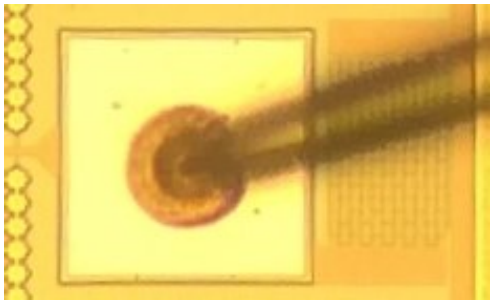

Fig. 8. Die microphotograph of the ESD structure in Fig. 6.

The following measurement has been logged with a LeCroy HD09104 at 4Gsa/s and shows the TLP pulse over a 50Ω load, where no reflection took place. Note the rise time 10% to 90%

is 0.990ns±0.267ns and the pulse width is 101.267ns±0.058ns over a set of 25 samples.

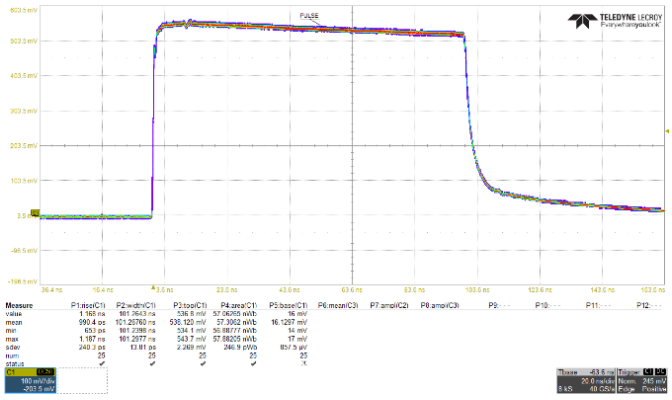

Fig. 9. TLP pulse measurement over a 50Ω load.

The I-V results of the TLP tests are shown in the following figure.

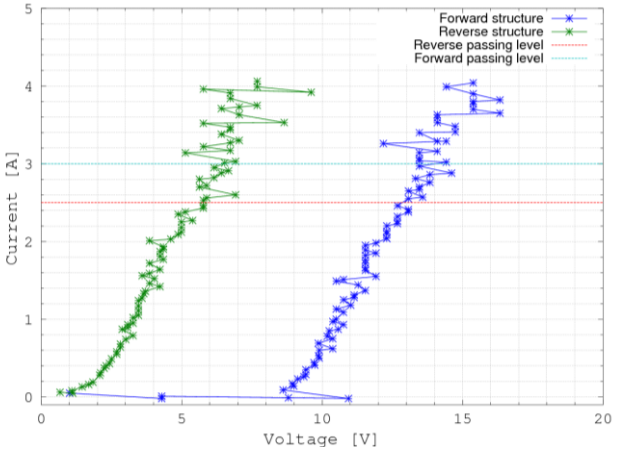

Fig. 10. Forward and reverse TLP I-V plot of the GGNMOS.

In the I-V curves it is seen that the reverse protection is achieving a 2.5A level while the forward is achieving 3.0A, which correspond to -3700V and +4500V, respectively, in the HBM standard (1.5kΩ, 100pF). Leakage current was the criteria to determine the failure mode.

Other standards such as the International Electrotechnical Committee (IEC) 61000-4-2 standard have not been tested due to the requirement of an ESD tester.

V. Conclusions

The design of ESD protection structures for biomedical applications have been presented including both design and layout guidelines. The performance has been successfully characterized based on a cost-effective TDR approach that guarantees the structures are reaching at least ±3700V in the Human-Body Model.

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