Application of Robust Control to a Cryogenic Current Comparator

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***Abstract* — We describe the design and implementation of an H_∞ controller for PTB's 14-bit cryogenic current comparator (CCC). Measurement results obtained using either the newly implemented digital H_∞ controller or the conventional analog integrator are consistent. In a wide frequency range, the system's noise figure is improved when using the new controller.**

I. Introduction

Running a CCC-based resistance measurement bridge requi-res the operation of the magnetic sensor, a SQUID, in a flux-locked loop regime. Specific demands on the control to be established result from features of the SQUID, especially from the possibility of "flux jumps" along the periodic flux-voltage characteristic, as well as from the fact that CCC windings have to be included into the feedback loop. Hence, self-reso-nances in the CCC, as typically found in the frequency range from several hundreds of Hz up to a few tens of kHz, will im-pose constraints. Moreover, the frequency dependence of SQUID output might vary with the combination of resistors to be compared and the numbers of turns of the CCC windings used. In PTB's CCC setup, stability of the flux-locked loop for very different application-specific configurations is achieved using an analog integrator of adjustable gain.

From the point of view of control theory, this straightforward solution represents the simplest scheme. Nowadays, more elaborate approaches are well-established. We consider the CCC-based measurement bridge as an interesting object for the application of the concept of robust control in metrology (cf. Ref. [1] and references therein). In this contribution we will deal with the implementation of an H_∞ controller [2].

II. Robust Controller Implementation

A. Setup

Besides the resistors to be compared, the setup considered here consists of PTB's home-made 14-bit CCC probe equipped with a dc-SQUID (cf. Ref. [3]) and operated with a commercial CCC or SQUID electronics, respectively [4]. This system is highly flexible by design and offers easy access to the electrical signals at relevant nodes. Especially, the optical isolation stage usually used for supplying one of the current sources with the feedback signal (so far: from the output of the analog integrator), is of interest here. In the following it will be used to perform transfer function measurements as well as to include another controller besides the established analog integrator. Fig. 1 shows a schematic diagram.

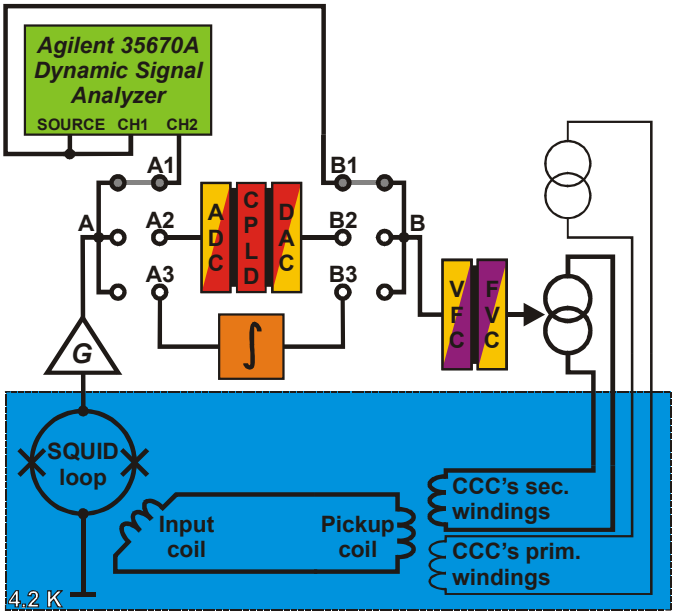

Fig. 1. Simplified scheme of the control loop including an amplifier of fixed gain *G*, and voltage-to-frequency and frequency-to-voltage converters (VFC resp. FVC). For recording the frequency response in open-loop configuration, **A** and **B** have to be connected via **A1**–**B1** (shown in grey color). Connection via **A2**–**B2** corresponds to the closed-loop operation using the digital controller consisting of analog-to-digital and digital-to-analog converters (ADC resp. DAC) with a complex programmable logical device (CPLD) in between. Connection via **A3**–**B3** corresponds to the use of an analog integrator.

B. Identification and Controller Design

Identification of the system starts with recording the frequency response in open-loop operation. This is done in the **A–A1–B1–B** configuration of the setup shown in Fig. 1. Based on these data, a model of the transfer function from the

secondary current source to the SQUID output is derived and then used for designing an appropriate controller. Note that the identification and subsequent steps are done for frequencies up to only 10 kHz, a limit which is set by the VFC–FVC module.

C. Hardware of the Digital Control Unit

The amplified SQUID output voltage is sampled using an 18-bit successive approximation register ADC. This is followed by the CPLD used for the calculation of the (digital) feedback signal. Finally, the CPLD output is converted into an analog signal by a 20-bit DAC.

Each of the converters operating at a sampling frequency of 100 kHz was mounted onto its individual Eurocard board including an isolated serial interface, a voltage reference and a signal conditioning circuit. Analog low-pass filters with cut-off frequencies of 15 kHz and 100 kHz were implemented before the ADC or after the DAC, respectively. For digital data processing, we used a CPLD from the Altera MAX II family (model EPM1270F256C5) with a clock frequency of 66 MHz.

In addition to the finite resolution of ADC and DAC, CPLD-related limitations of the performance have to be analyzed. The control law calculation performed in the CPLD is based on difference equations. The original result of the controller design is a set of floating point numbers. However, these coefficients – the numerical representation of the controller – have to enter the CPLD calculation as fixed-point numbers with a (max.) length of 20-bit. This conversion potentially affects the controller's pole frequencies and, hence, the closed-loop stability. Internally, the CPLD works with a single 20-bit multiplier and a 40-bit accumulator. The finite resolution in calculation will cause rounding errors with the consequences exemplarily demonstrated in the next section. In addition, the limited number of logic elements (1270) restricts the program to the implementation of a controller up to 4th order.

III. Results and Conclusions

As an example, we present in this contribution our investigation of the bridge setup when comparing two normal resistors of nominal values 12.9 kΩ and 100 Ω in the very same configuration. Once the digital controller has been designed and implemented, we performed a series of successive measurements using this and the analog controller alternately (**A2–B2** or **A3–B3**, respectively, in Fig. 1). The results obtained for the average bridge voltage difference and, hence, for the final resistance ratio, agree within the standard uncertainty which is in the order of one part in 10^9. We observed that the experimental type-A uncertainty is slightly lower when using the integral controller, especially in high-value resistance measurements. Accordingly, the flux noise in the SQUID loop at the given current reversal frequency of 50 mHz seems to be less efficiently suppressed with the H_∞ controller than with the analog integrator. Instead, for frequencies from about 30 Hz to 1 kHz, the SQUID noise spectral density in closed-loop configuration reveals superior performance of the digital controller as shown in Fig. 2. From these data we conclude that the setup will be more robust against distortions in this frequency range, an example is given in Ref. [5]. Moreover, the limitation of feedback bandwidth set by the CCC's self-resonance, which is generally found for the integrative controller, can be overcome when using the digital H_∞ controller.

In view of the limitations mentioned in the preceding subsection, we separately investigated the influence of the multiplier's bit length. We deliberately reduced this parameter to 18-bit and even 17-bit. The cancellation of SQUID noise remained superior at frequencies down to about 100 or 150 Hz, respectively, but at still lower frequencies, it leveled off resulting in an increasing deviation of the average bridge voltage difference from the value found with the integrative controller and the full 20-bit version of the digital controller.

Altogether, we see room for further improvement of the digital controller's implementation and overall performance. Besides an increase of the ADC and DAC's resolution, a replacement of the CPLD by a state-of-the-art field programmable gate array (FPGA) could provide new possibilities.

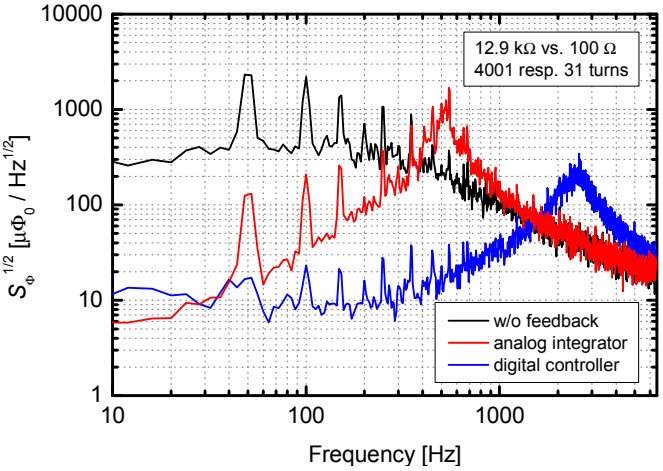

Fig. 2. Spectral density of the flux noise in the SQUID loop as a function of frequency.

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