Power Supply Rejection and Sensitivity Analyses of a Peak Current Source with Emitter Degeneration

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***Abstract*—Technology developments are demanding increasingly stringent requirements in terms of Electromagnetic Compatibility (EMC). For IC designers, this implies increasing Power Supply Rejection (PSR) while at the same time reducing the Icc spectrum. This work provides a theoretical analysis of the Peak Current Source with emitter degeneration (PCS-ED), a well known current mirror to achieve high PSR, which gets improved even further by the emitter resistance. The trade-off between the output current and the PSR were analyzed, as well as a sensitivity analysis to quantify the effects of the emitter degeneration. Experimental measurements have been performed to validate the immunity of an off-the-shelf bipolar transistor array from 100kHz up to 1GHz. Results showed that despite the small-signal analyses predicted a considerable improvement, the non-linear effects introduced by the input stage remained as the limiting factor in terms of PSR, leading to similar responses in the Peak Current Source (PCS) and the PCS-ED, despite one having much larger PSR than the other.**

***Index Terms*—Reference current source, Peaking current source, Nagata current source, Electromagnetic Compatibility, Sensitivity, Emitter Degeneration, Power Supply Rejection**

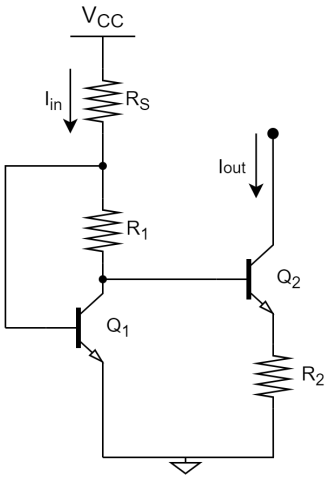

Fig. 1. Peak Current Source with Emitter Degeneration (PCS-ED).

I. Introduction

In recent years, ElectroMagnetic Compatibility (EMC) has become substantially important in the semiconductor industry, especially in the automotive market [1], where the developments towards the Electric Vehicle (EV), the Hybrid Electric Vehicle (HEV) and the Advanced Driver Assistance Systems (ADAS), among many others, are demanding increasingly stringent requirements in terms of EMC [2].

These requirements such as the ISO 11541-2 [3] are usually performed at the Vehicle Level prior to market release and they are, expectedly, called Final Compliance tests. Nevertheless, the automotive companies need to have confidence that the product they are currently designing is going to meet these standards once the vehicle is fully assembled. Therefore, they request from their suppliers, the automotive part manufacturers, some equivalent tests. These tests are usually called Pre-Compliance tests and instead of evaluating the entire vehicle, they are performed in a reduced sub-system and therefore they are also known as System-level tests. Example of these ones are the Bulk Current Injection (BCI) test from the ISO 11452-4 [4] and both Conducted Emissions (CE) and Radiated Emissions (RE) from the CISPR 25 [5].

In addition to that, the complexity of nowadays electronic automotive systems forces the auto part companies to have their own suppliers, the Integrated Circuit (IC) manufacturers. Following the chain of requirements, ICs must meet some equivalent EMC tests to guarantee, later on, the expected performance at the System and Vehicle levels. Examples of these IC-level tests are Direct Power Injection (DPI) from the IEC 62132-4 [6] and Direct Coupling Method (DCM) from the IEC 61967-4 [7]. If the IC does not comply with these EMC requirements, it cannot become a legally sold product.

Nowadays, the maximum frequency involved in DPI and DCM is 1 GHz. Therefore, an IC, whose largest geometry is the leadframe, which is not larger than 1 cm, can be considered electrically short and therefore modeled with the lumped

circuit theory [8]. This implies that the radiated immunity and emissions from the IC can be neglected as long as the operating frequencies remain reasonably low, compared with the electrically short hypothesis ($\lambda/20$) [8]. This implies that from an IC designer point of view, the EMC compliance can be reduced in DPI to an study of the immunity profile, aka Power Supply Rejection (PSR), and in DCM to the analysis of the Icc spectrum. Both on every pin.

When it comes to PSR, one of the most critical blocks is the regulator, which is usually built based on common blocks like bandgap references, current mirrors and operational amplifiers. Thus, the study of these fundamental blocks with especial emphasis on their PSR is of paramount interest in the semiconductor industry.

This work provides a theoretical analysis of the emitter degeneration of a discrete Peak Current Source (PCS) like the one presented in Fig. 1, a well known current mirror to achieve high PSR [9], which gets improved even further by the emitter resistance. In addition to that, this topology is also known to be highly sensitivity to process corners. Therefore, a sensitivity analysis has also been performed in the presence of the emitter degeneration to quantify the design trade-offs.

II. Circuit Analysis

The Peak or Peaking Current Source (PCS) was first invented by Minoru Nagata in 1966 [10] and modified in 1972 by M. T. Frederiksen [11]. Both designs have been the starting point for many circuit improvements and further studies [12]-[17], including circuit applications [18] - [20].

This topology has become a well-known current source because its PSR maximizes when Q_1 is biased in a specific Quiescent (Q) point given by the characteristic curve of Q_1 and R_1. This condition corresponds to the peak point in the response and it is generally achieved by setting $R_1 = V_T/I_{in}$ and $R_2 = 0\Omega$ [9]. When biased in this point, the current ratio becomes e^{-1} and that gives the circuit its name.

Despite the fact that this circuit has been extensively studied, the authors have not been able to find in the bibliography any quantitative nor qualitative analysis of the emitter degeneration. Taking into consideration the importance of PSR in nowadays electronics, an analysis of the degeneration of Q_2 becomes relevant.

The emitter resistance (R_2) provides, like any degeneration, increased noise rejection, output impedance, as well as an improvement on matching [21].

The transcendental equation that relates input and output currents in the PCS-ED is:

$$V_T \cdot ln\left(\frac{I_{in}}{I_{out}}\right) = I_{in}R_1 + I_{out}R_2 \tag{1}$$

where the input current is defined by:

$$I_{in} = \frac{V_{CC} - V_{BE}}{R_S} \tag{2}$$

In the following section, a sensitivity analysis will be developed using a small-signal hybrid model for Q_1 and Q_2.

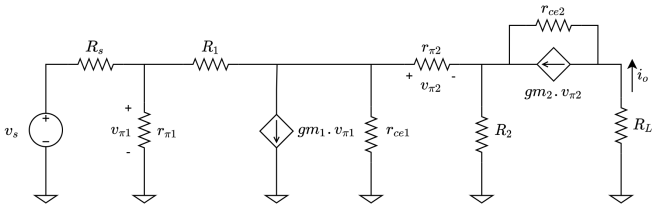

Fig. 2. BJT small signal model of PCS-ED.

The resistance R_s can be indistinctly considered as a physical resistor or as the small-signal resistance of a feeding current source.

From the small signal model in Fig. 2 without considering any of the noise sources, nor any intrinsic base resistance, and assuming R_s to be significantly larger than the dynamic resistance r_π, one may algebraically compute the dynamic output resistance as a function of R_2, the emitter resistance. Neglecting the mismatch between the transistors and assuming both to be operating at the same temperature, it can be shown that the dynamic output resistance R_o is given by the next expression:

$$R_o = \frac{\frac{r_{\pi1}+R_1}{1+gm_1 \cdot r_{\pi1}} + r_{\pi2}(1 + gm_2 \cdot r_{ce2}) + \left(r_{ce2}\frac{R_2(1+gm_2 \cdot r_{\pi2})}{R_1+r_{\pi1}}\right)}{1 + \frac{1}{R_1}\left(\frac{r_{\pi1}+R_1}{1+gm_1 \cdot r_{\pi1}} + r_{\pi2}\right)} \tag{3}$$

Where r_{ce2} denotes the collector-emitter dynamic resistance of the output transistor and R_2 boosts R_o as expected.

A. Sensitivity Analysis

In order to quantify the improvements of the emitter degeneration, this section analyzes the sensitivity of the output current (I_{out}) to power supply variations (V_{cc}).

$$S_{V_{cc}}^{I_{out}} = \frac{V_{cc}}{I_{out}} \cdot \frac{\partial I_{out}}{\partial V_{cc}} \tag{4}$$

Applying (4) into (1) leads to the following equation.

$$S_{V_{CC}}^{I_{out}}|_{PCS-ED} = \left(\frac{1 - \frac{I_{in}.R_1}{V_T}}{1 + \frac{I_{out}.R_2}{V_T}}\right).S_{V_{CC}}^{I_{in}} \tag{5}$$

Setting $R_2 = 0\Omega$ gives the sensitivity for the PCS.

$$S_{V_{CC}}^{I_{out}}|_{PCS} = \left(1 - \frac{I_{in}.R_1}{V_T}\right).S_{V_{CC}}^{I_{in}} \tag{6}$$

Where

$$S_{V_{CC}}^{I_{in}} = \frac{I_{out}}{I_{in}} \cdot \frac{\partial I_{in}}{\partial V_{cc}} \tag{7}$$

Notice that since (5) is divided by a factor larger than one, the sensitivity is improved by the emitter resistance. Fig. 3 shows the sensitivity as a function of R_2, with the PCS-ED biased at a point 20% away from its expected value at

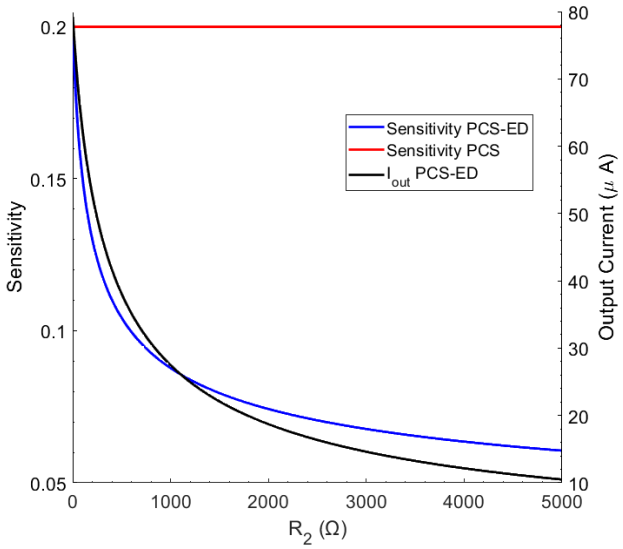

Fig. 3. $S_{V_{CC}}^{I_{out}}$ as a function of R_2.

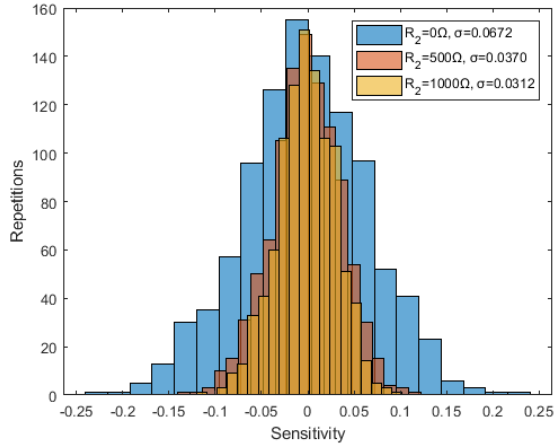

Fig. 4. Histograms of $S_{V_{CC}}^{I_{out}}$ taking a random Gaussian distribution for R_1.

the peak point. It is interesting to note that there is a point where the increase of R_2 stops being effective for reducing the sensitivity. Moreover, it can be showed based on (1) that increasing R_2 also reduces I_{out}, compromising the usefulness of the source.

Alternatively, Fig. 4 shows the reduction in the spread of the sensitivity between the PCS and the PCS-ED, as well as the limit of that improvement ($R_2 = 500\Omega$ and $R_2 = 1k\Omega$ lead to practically the same distribution). Adding the emitter resistance considerably improves $S_{V_{CC}}^{I_{out}}$, but as R_2 keeps increasing, the benefit becomes less significant.

For example, $R_2 = 600\Omega$ halves the sensitivity while reducing the current from $80\mu A$ to $35.4\mu A$. However, to halve the sensitivity again, R_2 needs to become larger than $5k\Omega$, making the current closer to $10\mu A$.

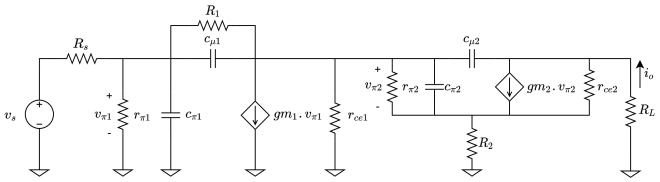

Fig. 5. BJT High frequency model of PCS-ED

B. Frequency Response Analysis

It is now of interest to find a theoretical approximation to the frequency response of the circuit, using the Zero Value Time-constants (ZVT) method [22]. Because the output transistor is in a common-emitter configuration, the equivalent base-collector capacitance of such transistor ($C_{\mu 2}$ in Fig. 5) will be amplified by the Miller effect. Therefore, the model can be further simplified by assuming that the time constant associated with $C_{\mu 2}$ will dominate over the others, and thus, the overall response will be that of a first-order system.

Neglecting the intrinsic base resistances, the time constant $\tau_{\mu 2}$ associated with $C_{\mu 2}$ is:

$$\tau_{\mu 2} = C_{\mu 2} \cdot R_{\mu 2} \tag{8}$$

Where $R_{\mu 2}$ denotes the equivalent dynamic resistance seen by $C_{\mu 2}$, which is approximated by the following expression:

$$R_{\mu 2} \cong \left(1 + \frac{gm_2 \cdot r_{\pi 2} \cdot R_L}{r_{\pi 2} + (1 + gm_2 \cdot r_{\pi 2}) \cdot R_2}\right) \cdot R_D \tag{9}$$

Where R_D is given by:

$$R_D = (R_{o1} || (r_{\pi 2} + (1 + gm_2 \cdot r_{\pi 2}) \cdot R_2)) \tag{10}$$

In this last equation R_{o1} refers to the dynamic output impedance of the transistor Q_1 and is likewise given by:

$$R_{o1} = \frac{1 - \dfrac{g_{m1} r_{\pi 1}^*}{1 + g_{m1} r_{\pi 1}^*}}{\dfrac{1}{r_{o1}} + \dfrac{1}{R_1 + (R_s \parallel (r_{x1} + r_{\pi 1}))}} \tag{11}$$

In order to verify the validity of the model just derived, the frequency response of the circuit is simulated using NGSPICE, and the results compared with those predicted by the theoretical model. The comparison is showed in Fig. 6.

Note for $R_2 = 0\Omega$, despite a second pole appearing due to $C_{\pi 1}$ and $C_{\pi 2}$, the first order ZVT model is an accurate description of the circuit up to 200 MHz.

For larger values of R_2, the output current is reduced, making the g_m of Q_2 lower, whereas the dynamic output resistance increases. Not only does that increase the bandwidth due to the overall lower Miller effect (which is not desirable in terms of PSR), but also the Right-Half Plane (RHP) Zero introduced by the feed-forward path of $C_{\mu 2}$ starts to show up. This is another side-effect of the emitter degeneration. It is worth mentioning that these singularities can eventually be canceled out (similar to the situation with $R_2 = 1k\Omega$).

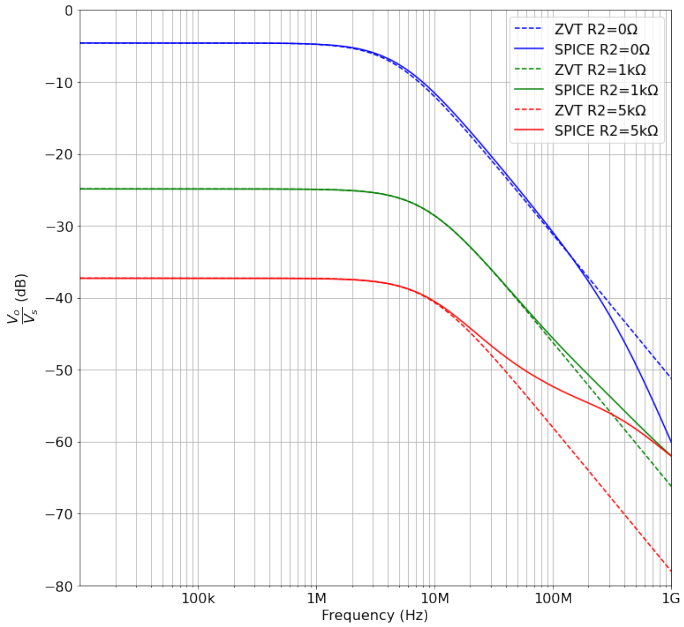

Fig. 6. Frequency response validation.

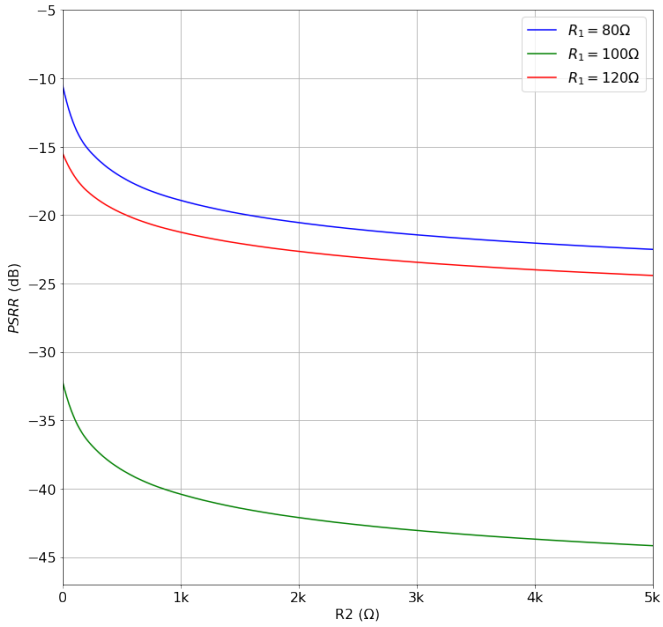

Fig. 7. Small signal PSRR simulations.

All in all, despite the fact that the attenuation over frequency becomes compromised due to the aforementioned effects, the low frequency PSR improvement is large enough to deal with such deviations (in Fig. 6, the red curve is always below or equal to the others up to 1GHz).

C. PSRR Analysis

This section covers the Power Supply Rejection Ratio (PSRR) simulation of the PCS and the PCS-ED. To quantify the results, the following definition of PSRR was used:

$$PSRR = 20 \cdot log_{10}\left(S_{V_{CC}}^{I_{out}}\right) \tag{12}$$

Fig. 7 shows the PSRR results of the circuit presented in Fig. 1 following the previous definition. The enhancement of the PSRR when the circuit is biased in its optimum point correspond to the green curve. That curve exhibits a consistent improvement larger than 15 dB when compared with the other operating conditions. These variations correspond to the sensitivity of the PSRR to process corners ($\pm 20\%$ in R_1).

However, note that the benefits of the emitter degeneration can make the worst case PSRR of the PCS-ED larger than that of the PCS, even in the optimal operating condition. This confirms the advantage of the PCS-ED in terms of process variations.

III. Experimental Validation

A. Test-setup description

The PCS-ED is known for being typically biased with very low current, in the tens of nano-Ampere [9]. However, since measuring such levels of low current up to 1GHz was not doable with the available instruments, the proposed design deliberately introduced a higher current and a non-optimal bias (out of the peak). Despite not working at the optimal condition, the conclusions drawn from this work will still be applicable.

Defining $V_{CC} = 8.85V$, $R_S = 33k\Omega$ and $R_1 = 50\Omega$ halves the optimum input current up to $I_{in} \cong 246.9\mu A$ (considering $V_{BE_{(on)}} = 0.7V$). Resistance R_2 is swept from 0Ω to $5k\Omega$. The output current with this set of values goes from $I_{out} \cong 153\mu A$ with $R2 = 0$ to $I_{out} \cong 12.8\mu A$ with $R_2 = 5k\Omega$. The circuit was implemented using an off-the-shelf monolithic NPN transistor array (LM3046).

Last but not least, in order to inject the AC disturbance, an RF generator NSG4070C and an RF Amplifier SMX100 have been used. The RF schematic showed in Fig. 8 has been designed to deliver the power up to the circuit in an efficient manner. The goal of the peripheral circuitry is to provide a low impedance path between the RF amplifier and the circuit under test, while at the same time provide the DC supply to the circuit. For doing that a Bias Tee composed by C_1, F_1, R_3 and C_2 has been designed.

The AC voltage developed across Vcc and Gnd during the RF power injection has been estimated from the built-in power-meter unit of the RF generator and converted to voltage by the impedance presented by the circuit, which was measured with a Network Analyzer PicoVNA 106.

The test performed is based upon DPI [6]. The input power is increased until some quantity exhibited a failure. In this case the failure mode was the DC shift on the output current, which was limited to $\pm 2\%$. This failure mode is one of the most common types for these current mirror-like structures [8]. In other words, if the quiescent output current were $100\mu A$, the RF power at a certain frequency was increased until the mean value of the output current shifted more than $\pm 2\mu A$.

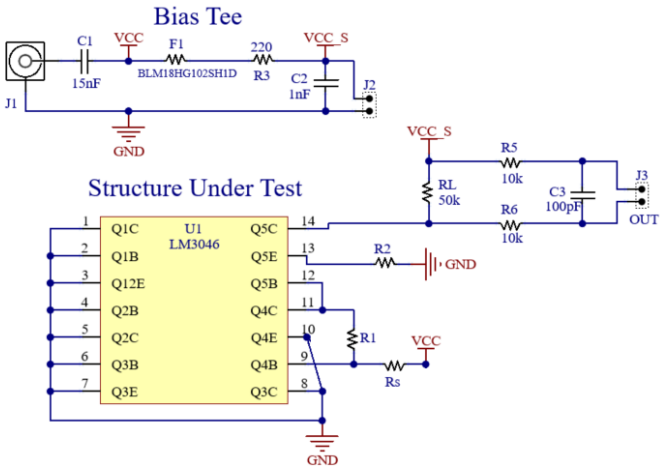

Fig. 8. Schematic of the PCB employed for the PSR analysis.

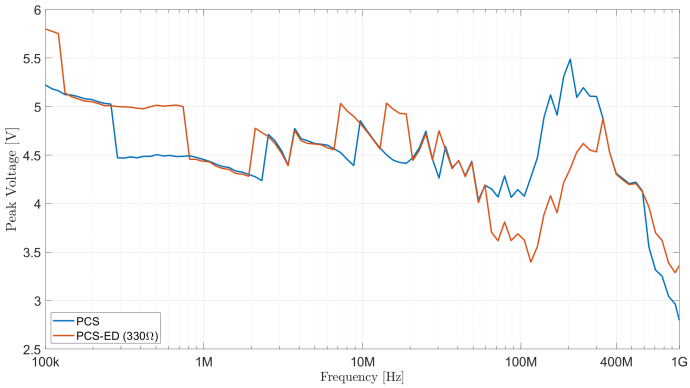

Fig. 9. Maximum peak voltage of the EMI signal without violating the failure criteria. The step resolution of the RF generator was 1 dB.

B. Test Results

The results of the DPI-like test are shown in Fig. 9 and the levels of output current for such disturbance are presented afterwards in Fig. 10. Fig. 11 shows a scope capture taken during the test. The current was estimated by measuring the single-ended voltages because the CM voltage exceeded the limit of the differential active probes available.

Even though the PSR analysis shown before predicted a considerably improvement on the PCS-ED, the results of Fig. 9 show that up to 60 MHz the PCS-ED has equal or slightly better performance than the PCS. Between 60 MHz and 600 MHz, the PCS is able to withstand larger amplitudes of EMI than the PCS-ED and beyond that, the PCS-ED is slightly better than the PCS.

This discrepancy with the PSRR analysis shown before can be explained by identifying the limiting factor of the circuit. The emitter degeneration increases the PSRR by acting on the output transistor (Q2). However, the DC shift observed in the output is produced in the input transistor (Q1).

Therefore, since the limiting factor is the dynamic range of the input stage, the benefit of the degeneration is not seen from the point of view of the immunity against EMI on Vcc.

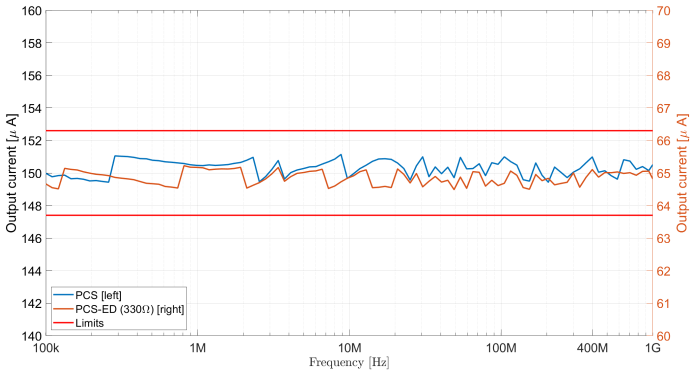

Fig. 10. Output current of the source during the test for the maximum level of disturbance reported in Fig. 9.

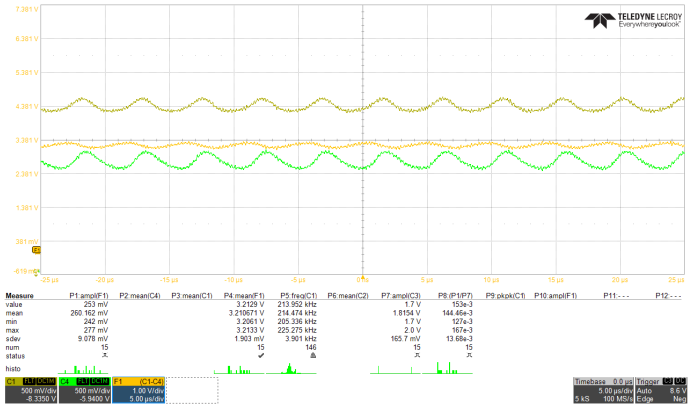

Fig. 11. Scope capture during the test showing the non-linear behavior of the source.

IV. Conclusion

This work has demonstrated that the emitter degeneration of the PCS can reduce the sensitivity of the output current to power-supply variations at the expense of a reduced output current, especially for increasing values of emitter resistance.

In addition to that, the bandwidth of the source is also increased for larger values of the emitter resistance (which is a non-desirable feature in terms of EMC). However, as it was shown in the frequency response analysis, the low frequency improvements on the response introduced by the emitter degeneration compensate the reduced attenuation due to the larger bandwidth and the RHP-zero.

Last but not least, in a real-life condition that was tested following an approach similar to DPI [6], the PSRR of the PCS and the PCS-ED have been pretty much identical. The main difference with the AC analysis that predicted a much larger PSRR for the PCS-ED was that in such analysis large-signal effects like DC shift were not under consideration. Nevertheless, as long as the levels of disturbance do not compromise the input dynamic range and the baseline noise does not exceed the EMI, the PSRR benefits of the PCS-ED are still applicable.

REFERENCES

[1] German National Platform for Electric Mobility (NPE) , "The German Standardisation Roadmap Electric Mobility 2020", Federal Government's Joint Office for Electric Mobility (GGEMO), Berlin, April, 2017.

[2] T. Steinecke et al., "Generic IC EMC Test Specification", *Asia-Pacific Symposium on Electromagnetic Compatibility*, pp. 5-8, 2012.

[3] ISO 11451-2 (2015): Road vehicles — Vehicle test methods for electrical disturbances from narrowband radiated electromagnetic energy — Part 2: Off-vehicle radiation sources, Ed. 4.

[4] ISO 11452-4 (2020): Road Vehicles-Component Test Methods for Electrical Disturbances by Narrowband Radiated Electromagnetic Energy Part 4: Bulk Current Injection (BCI), Ed. 5

[5] CISPR 25 (2016): Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers, Ed. 4

[6] IEC 62132-4, "Integrated circuits - Measurement of Electromagnetic Immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method", Ed. 1, 2006

[7] IEC 61967-4, "Integrated Circuits - Measurements of Electromagnetic Emission, 150 kHz to 1 GHz — Part 4: Measurement of Conducted emission - $1\Omega/150\Omega$ Direct Coupling Method", Ed. , 2006

[8] Redouté, J.-M., Steyaert, M. (2010): *EMC of analog integrated circuits*. ISBN: 978-90-481-3229-4. New York: Springer.

[9] P. R. Gray and R. G. Meyer, *Analysis and design of analog integrated circuits*. New York: Wiley, 1977. 46-16463 (Dec. 12, 1966).

[10] Inventor M. Nagata, Japanese Patent, Showa 46-16463 (Dec. 12, 1966)

[11] T. M. Frederiksen, "Constant current source" U.S. Patent 3 659 121, Apr. 25, 1972.

[12] V. Gheorghiu and A. A. Vild-Major, "Optimum design of two cascaded peaking current sources," in *IEEE Journal of Solid-State Circuits*, vol. 16, no. 4, pp. 415-417, Aug. 1981

[13] M. S. Eslampanah, S. Kananian, M. Sharifkhani, and A. M. Sodagar, "Temperature Compensation in CMOS Peaking Current References," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1139–1143, Sept 2018.

[14] D. V. Kerns, "Optimization of the peaking current source," in *IEEE Journal of Solid-State Circuits*, vol. 21, no. 4, pp. 587-590, Aug. 1986

[15] D. V. Kerns, "Enhanced peaking current reference," in *IEEE Journal of Solid-State Circuits*, vol. 23, no. 3, pp. 869-872, June 1988.

[16] Cheng, M.-H.; Wu, Z.-W. (2005). "Low-power low-voltage reference using peaking current mirror circuit." *Electronics Letters*, 41(10), 572.

[17] M. Hirano, N. Tsukiji and H. Kobayashi, "Simple reference current source insensitive to power supply voltage variation - improved Minoru Nagata current source," *13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2016.

[18] K. Fukahori, Y. Nishikawa and A. R. Hamade, "A high precision micropower operational amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 14, no. 6, pp. 1048-1058, Dec. 1979

[19] C. Y. Kwok, "Low-voltage peaking complementary current generator," in *IEEE Journal of Solid-State Circuits*, vol. 20, no. 3, pp. 816-818, June 1985.

[20] K. Kimura, "Low voltage techniques for bias circuits," in *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 5, pp. 459-465, May 1997.

[21] A. Bilotti, E. Mariani, "Noise characteristics of current mirror sinks/sources" *IEEE Journal of Solid-State Circuits*, vol. SC-10, no. 6, pp. 516–524, Dec 1975.

[22] A. Hajimiri, "Generalized Time- and Transfer-Constant Circuit Analysis" *IEEE Transactions on Circuits and Systems—I*, vol. 57, no. 6, June 2010.