A Chopped Front-End System with Common-Mode Feedback for real time ECG applications

Gardella, Pablo, *Member, IEEE,* Villa Fernandez, Emanuel, *Student Member, IEEE,*
Baez, Eduardo, Cesaretti, Juan M., *Member, IEEE*
Electronic Engineering Department
Instituto Tecnológico de Buenos Aires (ITBA)
Buenos Aires, Argentina
Email: pgardell@itba.edu.ar, evillafe@itba.edu.ar, ebaez@itba.edu.ar, jcesaret@itba.edu.ar

***Abstract*—A Front-End system composed of an instrumentation amplifier with common-mode feedback and a second-order sigma-delta analog to digital converter is proposed. Chopping techniques are used to remove offset and low-frequency noise to guarantee a noise floor below the signal of interest. Measurements show that common-mode feedback adds 71 dB to the CMRR at 50 Hz and the input referred noise is 1.17 μV_{RMS} over the frequency range of 0.1 Hz to 400 Hz.**

Keywords—Chopper amplifier, Common-mode feedback, Instrumentation Amplifier, CMRR, ECG

I. INTRODUCTION

Physiological monitoring devices are becoming an important research topic in biomedical electronic systems. Electrocardiogram (ECG), electroencephalogram (EEG) and oxygen saturation in blood are some of the most common extracted parameters [1]. The performance of these systems is limited by offset and flicker noise at the Front-End Amplifier. Also of importance is high common-mode rejection ratio (CMRR), required to attenuate large input common-mode signals (in particular 50/60 Hz AC line) while simultaneously amplifying the differential signal of interest.

Some state of the art approaches to achieve low noise are based on subthreshold biased gm-C filters [2, 3]. Although this technique can achieve promising results, their limited linearity under CMOS process variations restricts their usefulness. Other schemes propose passive off-chip filters, as in [4]. In this work, a chopped Instrumentation Amplifier (IA) is implemented to overcome this difficulty [5-7].

The proposed system is presented in Fig. 1. It is composed of an IA, followed by a second order Sigma-Delta Analog to Digital Converter and a Common-Mode Feedback Loop. Offset and flicker noise in the signal path are removed via a chopping scheme implemented on the IA [5], while CMRR is improved using a feedback loop through the patient's body as in [8].

This paper is structured as follows. Section II covers the design and implementation of the ECG measurement system. Subsections are dedicated to the Front-End Instrumentation Amplifier, the common-mode feedback circuit and the analog to digital converter. Measurements are presented in section III, while conclusions are presented in section IV.

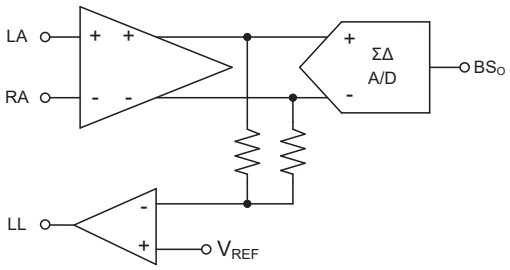

Fig. 1. Simplified architecture of the proposed ECG acquisition system.

II. DESIGN AND IMPLEMENTATION

The characteristics of the ECG signal must be well understood to properly design the amplification and processing system. The deflections of an ECG signal are usually labeled as P, Q, R, S and T, as shown in Fig. 2.

The QRS complex is usually the largest signal feature, with a peak value up to 5 mV. Conversely, the P wave is the smallest feature, with a peak value in the order of 200 µV [9]. The detection error should be below 10 µV [10]. As a reference, 25 µV is usually the smallest noticeable feature on a paper based ECG [11].

The American Heart association recommends a minimum signal bandwidth of 150 Hz, but for pediatric studies the bandwidth should be increased to at least 250 Hz [11]. The low frequency limit is generally set at 0.05 Hz, but can be increased to 0.67 Hz if linear digital filters with zero phase distortion are used [12]. In order to capture higher frequency content (relevant in some applications) the system bandwidth for the project is thus defined from 0.1 Hz to 400 Hz. Filtering is to be implemented on the digital domain. In table I, minimum and maximum ECG's signal amplitude and frequency content are presented.

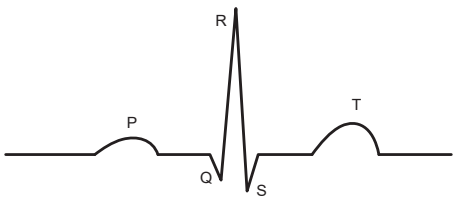

Fig. 2. Simplified representation of a normal sinus rhythm ECG.

TABLE I. INPUT SIGNAL CHARACTERISTICS

ECG	***Minimum***	***Maximum***
Amplitude	10 µV	5 mV
Bandwidth	0.1 Hz	400 Hz

A. Front-End Amplifier

The front-end subsystem consists of an Instrumentation Amplifier (IA) and a common mode feedback block. A schematic diagram of the IA is shown in Fig. 3.

ECG signal wander (due to, for example, sudden physical movements) and offset between the input electrodes (small electrical voltages in the body) are seen by the amplifier as differential signals (as high as 10 to 20 mV). They can be digitally removed, but care must be taken in order not to saturate the signal path. For this reason, the amplifier gain is limited to x100.

Offset and flicker noise are a major concern on a pure CMOS process. A chopping scheme [6, 7] is thus implemented to modulate these components to higher frequencies.

Demodulation is performed in current mode before the amplifier's first stage high-impedance output node. The reason for this is twofold. First, it allows the chopping frequency not to be limited by the amplifier bandwidth; flicker noise content at higher frequencies can be removed. The second advantage is that the closed-loop amplifier bandwidth serves as a first order filter for the modulated offset and noise content. The chopping frequency has been set to 400 kHz, while the front-end amplifier bandwidth is 30 kHz.

The effect of the chopping mechanism can be clearly seen on Fig. 4. The simulated RMS input referred noise voltage in the band from 0.1 Hz to 400 Hz is 1.0 µV for the chopped amplifier and 10.7 µV for the unchopped version.

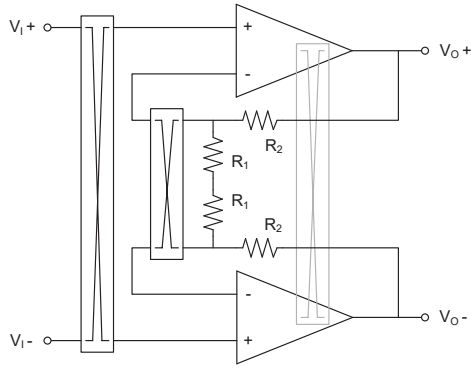

Fig. 3. Schematic representation of the instrumental amplifier.

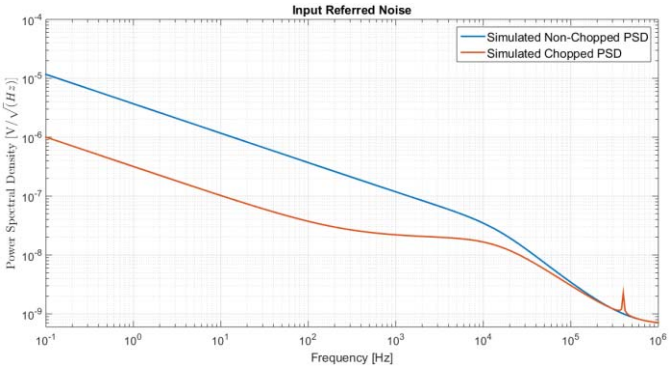

Fig. 4. Simulated input referred noise power spectral density.

To attenuate large input common-mode signals (in particular 50/60 Hz AC line) a good CMRR is important. In traditional IA topologies, CMRR is highly dependent on resistor's matching [8], which is difficult to achieve due to variations in the CMOS process technology. To improve this figure, different techniques such as Faraday shielding [13], digital filtering [14] or common-mode feedback [8] can be implemented. This works implements the latter because it doesn't require external components nor the ECG signal is distorted due to filtering.

The feedback loop path consists of a high gain operational amplifier, the patient's body, the IA common-mode path and averaging resistors. The operational amplifier is connected to patient's left leg, and the applied voltage is picked up by the left and right arm's electrodes. The common-mode signal traverses the IA with unity gain and is afterwards compared with a reference input.

The consequence of this loop is that any low frequency common-mode disturbances present on the patient are effectively suppressed before entering the instrumental amplifier. Measurements on Section III confirm this assertion.

B. Sigma Delta Converter

A second-order, discrete time, single bit, sigma-delta analog to digital (ADC) converter is used to translate the amplified ECG signal to the digital domain. This type of ADC architecture is ideally suited to convert low frequency ECG signals to the digital domain. A second order topology was selected because it requires a lower sampling rate for the same SQNR compared to a first order topology. Also of concern is the first order topology propensity for idle-tone generation. The converter sampling frequency is set at 800 kHz, at double the IA chopping frequency. This frequency is high enough to provide a very good oversampling ratio, while not as high as to compromise the frequency response of the sigma-delta circuitry.

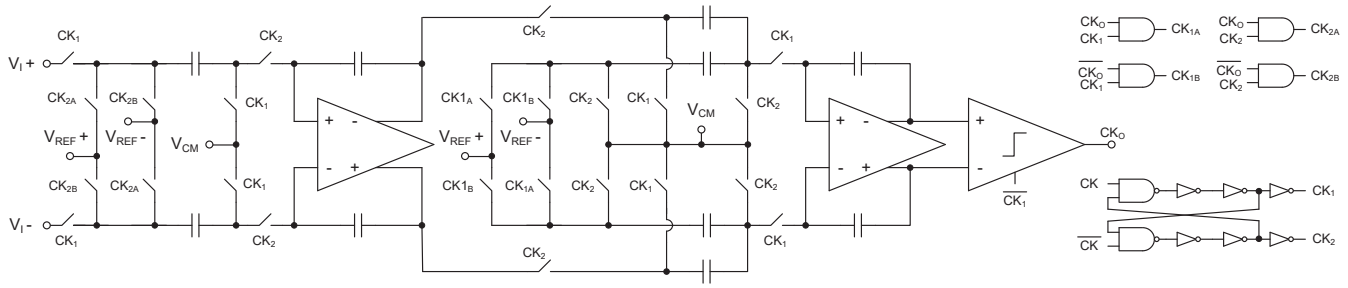

Fig. 5. Schematic representation of the sigma delta analog to digital converter

The sigma-delta ADC schematic diagram is depicted in Fig. 5. A Cascade of Integrators with distributed Feedback (CIFB) structure has been selected. The converter reference voltages have been defined as to allow up to a 3 V differential input signal. To avoid degradation in the converter performance, input signals should be kept well below this value. The input range is in accordance with Table I and with the effects of signal wander.

Quantization noise in the band of interest should be smaller than the IA's noise. The converter output spectrum is presented on Fig 6, where the 40 dB/decade noise shaping slope, characteristic of second order sigma-delta converters, can be clearly seen. The integrated noise in the band of interest is 2.70 µV (27 nV input referred).

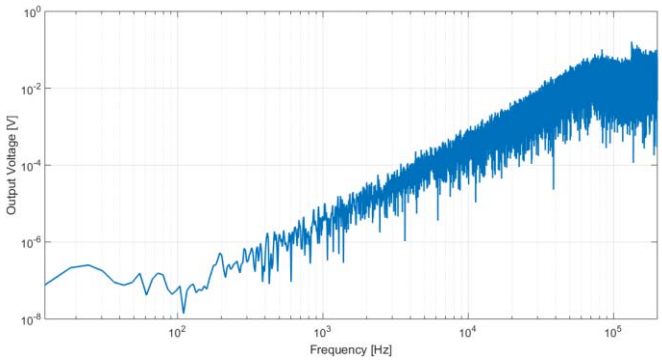

Fig. 6. Sigma-delta noise output spectrum.

C. *Auxiliary Blocks*

Supporting blocks have also been implemented in silicon. They include biasing circuitry (bandgap block, reference currents), a frequency oscillator, a digital cell library (created in-house) and ESD protection circuitry. For the latter GGNMOS protection structures were designed from scratch. Transmission-line pulse (TLP) testing has indicated the structures pass 1.5 A pulses, equivalent to 2 kV HBM.

III. EXPERIMENTAL RESULTS

The system has been implemented on a 0.6 µm CMOS process using MOSIS, a Multi-Project Wafer (MPW) service. A silicon microphotograph of the implemented circuits is shown in Fig. 7.

As part of the Instrumentation Amplifier evaluation, its noise spectral density has been measured. The results match very nicely with the expected response, as seen in Fig. 8.

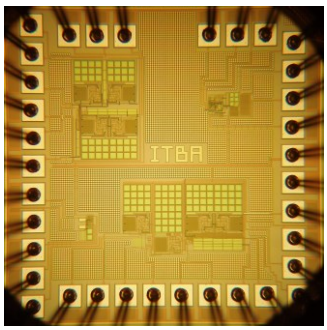

Fig. 7. Silicon die microphotograph.

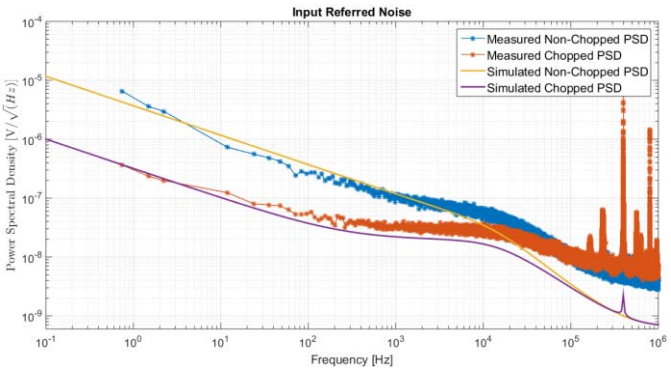

Fig. 8. Simulated and measured input referred noise PSD.

The measured RMS input referred noise voltage in the system's bandwidth is 10.10 µV (non-chopped) and 1.17 µV (chopped). The latter value is very close to the 1.0 µV obtained from simulations.

The expected CMRR at low frequencies with common-mode feedback active is 250 dB. Forcing the amplifier to a high swing (1V) output state (to drive the two internal operational amplifiers into dissimilar operating points) reduces the rejection to 140 dB. These values could not be experimentally validated. Forcing a 100 mV sinusoidal common-mode input yielded common-mode signals on the output differential channel too small to be detected with our equipment (LeCroy 606Zi).

A different approach was devised to evaluate the impact of common-mode feedback on CMRR. In a traditional IA architecture, the common-mode gain is equal to one. The addition of the feedback loop should reduce this gain considerably, thus also improving the CMRR.

Fig. 9 shows a comparison of simulated and measured common-mode gain responses with and without the common-mode feedback loop. Experimental results agree with their expected behavior. The common-mode gain reduction exhibits 71 dB of rejection at 50 Hz, hence considerably improving the CMRR of the instrumentation amplifier.

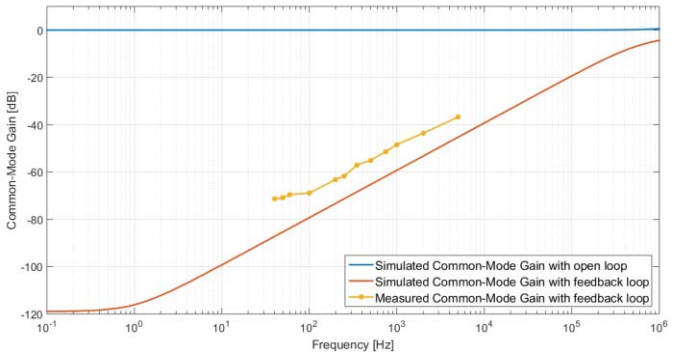

Fig. 9. Comparison of simulated and measured common-mode gain.

A recorded ECG signal from an adult patient is presented in Fig. 10. Typical deflections are identified. Even the smallest deflections (P, Q, and S) are clearly visible due to the low noise on the signal path. Moreover, the system bandwidth is high enough to amplify high frequency components (R) without any noticeable distortion.

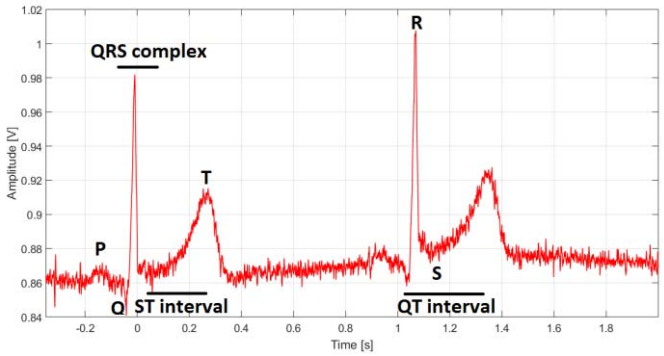

Fig. 10. Patient's ECG signal measured at IA's output.

IV. CONCLUSION

A chopped Instrumentation Amplifier with common-mode feedback was successfully implemented in a standard 0.6µm CMOS process technology. The measured detection error due to offset and flicker noise is 1.17 µV, which is far below the recommended value of 10µV [10]. Although a direct CMRR measurement was not possible, the common-mode feedback loop drastically reduces the common-mode gain, guaranteeing a good CMRR, comparable with the state of the art results shown in table II.

TABLE II. PERFORMANCE COMPARISON

	Noise Technique	CMRR	Bandwidth	Input Referred Noise	Process
[3]	gm-C filter	96 dB[a]	0.3-150 Hz	7.8 µV[a]	180 nm
[7]	Chopped	85 dB	0.5-10 kHz	5.7 µV	180 nm
[8]	gm-C filter	122 dB	0.05-125 Hz	2.3µV	180 nm
[15]	DC loop	73 dB	0.3-250 Hz	28.0 µV[a]	65 nm
This work	Chopped	140 dB[a]	0.1-400 Hz	1.2 µV	600 nm

a. simulated result

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