7-Level Asymmetric Multilevel Current Source Inverter with Predictive Control

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***Abstract*—In this paper a 7-Level Asymmetric Multilevel Current Source Inverter is presented. The topology considers two Current Source Inverters that follow a 1:2 ratio to generate the multilevel current waveform. A Model Predictive Control is used to track the internal current and voltage references as well as to keep the asymmetric ratio between the DC currents even during transient conditions. To properly use the predictive algorithm, the modelling equations of the presented topology are systematically obtained in continuous and discrete time domains, considering the characteristic constraints of a Current Source Inverter. Simulated dynamic tests are presented in order to prove the feasibility of the asymmetric approach and the properness of the predictive control technique.**

***Index Terms*—Model Predictive Control, Asymmetric Multilevel Inverters, Current Source Inverter.**

I. Introduction

The increasing demand of clean and cost-effective energy has led to propose different solutions in order to deliver power efficiently [1]. In this scenario, power electronics is playing an important role due to its capacity to convert energy from DC to AC, which is essential to integrate renewable energy sources to the existing facilities [2]. On the other hand, the use of multilevel converters has become the state-of-the art solution to overcome the power ratings limitation of the actual semiconductor devices, because they can generate high voltage and/or current AC waveforms using low power rated switches [3], [4]. As a drawback of the multilevel converters, dedicated control strategies are required to ensure the power balancing among the components, which makes control algorithms quite complex; however, this issue can be easily solved thanks to latest digital control boards available on the market, such as DSPs and FPGAs. [5], [6].

In recent years a novel technological trend has become quite popular related to the use of asymmetric multilevel converters. The main advantage of this approach lies in the higher number of levels that can be obtained with a reduced amount of switching devices. As the main drawback of this approach, compared with its symmetric counterpart, it is possible to mention the lack of modularity, i.e., if one cell fails (especially the higher power module) the topology is not able to work properly, as occur in conventional multilevel converters that use the $n+1$ reliability criterion [7].

The multilevel asymmetric approach has been well reported in literature for structures based on Voltage Source Inverters (VSIs), where the asymmetry ratios and the gating patterns have been optimized [8]. Furthermore, different control strategies and modulating techniques have been already addressed [9], [10]. Some applications of this kind of converters are also reported, where it is possible to highlight, motor drives [11], active power filters [12] and renewable energies integration [13], among others.

Although the asymmetric approach for multilevel converters was proposed several years ago [14], its implementation in topologies based on Current Source Inverters (CSIs) is limited. In fact, it is hard to find technical literature regarding this topic [15]. It is well known that CSC's have an important disadvantage related to their power losses [16]; however considering the asymmetric approach, it is possible to concentrate high amount of power in semiconductors with low switching frequency and therefore less power will be handled by the faster switching devices. This may allow to overcome the drawbacks of the CSCs, while it keeps the advantages, such as high reliability, fault tolerant operation, quasi soft switching and the use of capacitors of low value, among others [17], [18].

Regarding the state-of-the-art control techniques for multilevel converters, one of the most popular scheme since a couple of years ago is the Predictive Control, which has some advantages over linear control techniques, such as controllability range, dynamic response and the natural inclusion of nonlinear contraints [19]–[21].

In this paper, a 7-level Asymmetric Multilevel Current Source Inverter (AMCSI) is presented using two modules with a 1:2 ratio. The mathematical model is included and the valid states are depicted. The AMCSI is controlled with a predictive control scheme and simulated results are included in order to validate the proposal.

II. System Modelling

A. The Asymmetric Topology

The asymmetric multilevel inverter presented in this paper is shown in Fig. 1. It is composed of a voltage source, a current buck converter and two CSIs that feed a RLC three-phase load, where the capacitors act as passive filters aimed to smooth the voltage waveform and to filter-out current

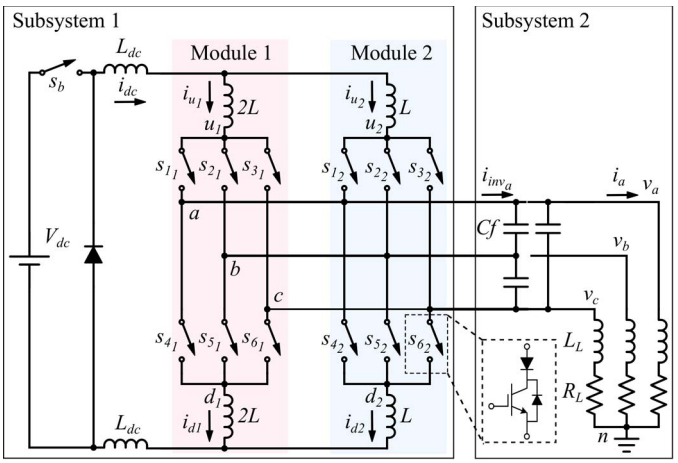

Fig. 1. Asymmetric Multilevel Current Source Inverter

switching harmonics generated by the inverter. The modules that compose the AMCSI are connected in parallel and the respective inductances follow the 1:2 ratio (L and $2L$), in order to generate the same asymmetry between the inverters currents. Both inverters are fed with a constant current set with the main inductance L_{dc}.

Similar to symmetric structures the power inverters consist of six reverse blocking switches that could be implemented with either insulated gate bipolar transistors (IGBT) each one with a series diode to block the reverse current or integrated gate commutated thyristors (IGCT), among others.

Thanks to the binary asymmetric ratio it is possible to generate up to 7 levels in the current waveform as explained in [22]. It is worth noting that, for the same number of levels, the symmetric approach would require three inverters, which considerably increases the complexity of the predictive control scheme, due to the higher number of combinations, as will be depicted hereafter.

B. Continuous-Time Model

The predictive control strategy requires the mathematical model of the entire system as well as all the valid states of the AMCSI. This is required in order to predict the future behaviour (in the next sampling time $k+1$) of the variables to be controlled, which in this case are the voltages in the AC side and the DC currents. As the asymmetric topology is based on CSIs, it is required to ensure that each module provides a valid path for the current, which is guaranteed only when one of the upper switches and one of the lower switches are closed in each inverter. This constraint can be mathematically expressed as

$$s_{1_\eta} + s_{2_\eta} + s_{3_\eta} = s_{4_\eta} + s_{5_\eta} + s_{6_\eta} = 1 \quad \eta \in \{1, 2\} \qquad (1)$$

where η is the module number. As expected, each CSI has nine valid states as depicted in TABLE I, where i_{a_η}, i_{b_η} and i_{c_η} are the output currents of each module and v_{ud} is the equivalent voltage between the terminals u and d of the module η. As the AMCSI considers two modules to generate 7 different levels of the output current, each one with 9 different valid states, there are $9^2 = 81$ possible combinations for the switches. Compared with its symmetric counterpart, in order to provide the same number of levels, it would be necessary the inclusion of a third inverter, which would produce $9^3 = 729$ valid states for the whole structure [23]. This feature allows to claim that the asymmetric approach can generate the same multilevel waveform that the symmetric multilevel inverter, but with substantially lesser number of valid states, which certainly facilitates the implementation of a predictive algorithm. On the other hand, as a drawback of this fact, it is possible to mention that the redundant states in the asymmetric approach are decreased, then the degrees of freedom of the control strategy are therefore limited.

TABLE I
OUTPUT CURRENT AND VOLTAGE v_{ud} OF MODULE η

State	s_{1_η}	s_{2_η}	s_{3_η}	s_{4_η}	s_{5_η}	s_{6_η}	i_{a_η}	i_{b_η}	i_{c_η}	v_{ud_η}
#1	1	0	0	1	0	0	i_{u_η}-i_{d_η}	0	0	0
#2	1	0	0	0	1	0	i_{u_η}	-i_{d_η}	0	v_{ab}
#3	1	0	0	0	0	1	i_{u_η}	0	-i_{d_η}	v_{ac}
#4	0	1	0	1	0	0	-i_{d_η}	i_{u_η}	0	v_{ba}
#5	0	1	0	0	1	0	0	i_{u_η}-i_{d_η}	0	0
#6	0	1	0	0	0	1	0	i_{u_η}	-i_{d_η}	v_{bc}
#7	0	0	1	1	0	0	-i_{d_η}	0	i_{u_η}	v_{ca}
#8	0	0	1	0	1	0	0	-i_{d_η}	i_{u_η}	v_{cb}
#9	0	0	1	0	0	1	0	0	i_{u_η}-i_{d_η}	0

In order to obtain the continuous-time system model, firstly the inverters and their respective current sources are modelled (Subsystem 1 in Fig. 1) using the valid states depicted in TABLE I and then, the differential equations that model the load dynamic behaviour are depicted (Subsystem 2 in Fig. 1). Therefore, in the first case, applying the Kirchoff laws, the modelling equations of the subsystem 1 are,

$$\begin{cases} i_{dc} & = i_{u_1} + i_{u_2} \\ i_{dc} & = i_{d_1} + i_{d_2} \\ V_{dc}\, s_b & = 2\, L_{dc}\, \dot{i_{dc}} + 2L\, \dot{i_{u_1}} + v_{un_1} + v_{nd_1} + 2L\, \dot{i_{d_1}} \\ V_{dc}\, s_b & = 2\, L_{dc}\, \dot{i_{dc}} + L\, \dot{i_{u_2}} + v_{un_2} + v_{nd_2} + L\, \dot{i_{d_2}} \\ V_{dc}\, s_b & = 2\, L_{dc}\, \dot{i_{dc}} + 2L\, \dot{i_{u_1}} + v_{un_1} + v_{nd_2} + L\, \dot{i_{d_2}} \end{cases} \qquad (2)$$

where s_b is the state of the switch of the buck converter that controls the current source. It can be observed form the first two equations that i_{dc} is linearly dependant on the CSIs currents, then it can be expressed in terms of i_{u_η} and i_{u_η}, which implies that i_{dc} is not considered a state variable of the system. On the other hand, voltages v_{un_η} and v_{nd_η} are the voltages between nodes u_η and n and between n and d_η, respectively. These voltages can be expressed as function of the switching signals s_{1-6_η} as,

$$\begin{bmatrix} v_{un_1} \\ v_{un_2} \end{bmatrix} = \begin{bmatrix} s_{1_1} & s_{2_1} & s_{3_1} \\ s_{1_2} & s_{2_2} & s_{3_2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$
$$\begin{bmatrix} v_{nd_1} \\ v_{nd_2} \end{bmatrix} = - \begin{bmatrix} s_{4_1} & s_{5_1} & s_{6_1} \\ s_{4_2} & s_{5_2} & s_{6_2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3)$$

The inverter output current i_{inv} for each phase is expressed in terms of the switching signals s_{1-6_η} as,

$$\begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \end{bmatrix} = \begin{bmatrix} s_{1_1} & s_{1_2} \\ s_{2_1} & s_{2_2} \\ s_{3_1} & s_{3_2} \end{bmatrix} \begin{bmatrix} i_{u_1} \\ i_{u_2} \end{bmatrix} - \begin{bmatrix} s_{4_1} & s_{4_2} \\ s_{5_1} & s_{5_2} \\ s_{6_1} & s_{6_2} \end{bmatrix} \begin{bmatrix} i_{d_1} \\ i_{d_2} \end{bmatrix} \quad (4)$$

Combining the last expressions, it is possible to obtain the state space representation of the first subsystem as

$$\begin{bmatrix} \dot{i}_{u_1} \\ \dot{i}_{u_2} \\ \dot{i}_{d_1} \\ \dot{i}_{d_2} \end{bmatrix} = a \begin{bmatrix} -c & d & -1 & -2 \\ d & e & -2 & -4 \\ -1 & -2 & -c & d \\ -2 & -4 & d & -e \end{bmatrix} \begin{bmatrix} v_{un_1} \\ v_{un_2} \\ v_{nd_1} \\ v_{nd_2} \end{bmatrix} + a\, s_b \begin{bmatrix} 3 \\ 6 \\ 3 \\ 6 \end{bmatrix} V_{dc} \quad (5)$$

where,

$$a = \frac{1}{6\,(2L + 3\,L_{dc})} \qquad b = 6\frac{L}{L_{dc}}$$
$$c = 5 + b \qquad d = 2 + b \qquad e = 8 + b \quad (6)$$

The capacitive filter as well as the resistive-inductive load that compose the second subsystem is modelled with,

$$\begin{cases} \dot{v_x} = \dfrac{i_{inv_x} - i_x}{3\,C_f} \\ \dot{i_x} = \dfrac{v_x - R_L\, i_x}{L_L} \end{cases} \quad x \in \{a, b, c\} \quad (7)$$

where C_f is the filter capacitance, L_L the load inductance and R_L the load resistance. In this case, the input of this subsystem, i_{inv_x} are generated as the output from subsystem 1. The state space representation for the presented equations is,

$$\begin{bmatrix} \dot{v}_a \\ \dot{v}_b \\ \dot{v}_c \\ \dot{i}_a \\ \dot{i}_b \\ \dot{i}_c \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & f & 0 & 0 \\ 0 & 0 & 0 & 0 & f & 0 \\ 0 & 0 & 0 & 0 & 0 & f \\ g & 0 & 0 & h & 0 & 0 \\ 0 & g & 0 & 0 & h & 0 \\ 0 & 0 & g & 0 & 0 & h \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ i_a \\ i_b \\ i_c \end{bmatrix} - f \begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (8)$$

where,

$$f = -\frac{1}{3\,C_f} \qquad g = \frac{1}{L_L} \qquad h = -gR_L \quad (9)$$

C. Discrete-Time Model

As thorougthly explained in technical literature [24], the predictive control requires the dynamic model expressed in the discrete-time domain. Therefore, this part is aimed to obtain a discrete representation of the afore-presented equations. To do so, the forward Euler transformation is used, which considers the derivative of a generic variable s as

$$\frac{ds}{dt} = \frac{s_{k+1} - s_k}{T_s} \quad (10)$$

where T_s is the sampling time. Then, using this last equation to discretize the model in (5), (11) is obtained,

$$\begin{bmatrix} i_{u_1} \\ i_{u_2} \\ i_{d_1} \\ i_{d_2} \end{bmatrix}_{k+1} = aT_s \begin{bmatrix} -c & d & -1 & -2 \\ d & e & -2 & -4 \\ -1 & -2 & -c & d \\ -2 & -4 & d & -e \end{bmatrix} \begin{bmatrix} v_{un_1} \\ v_{un_2} \\ v_{nd_1} \\ v_{nd_2} \end{bmatrix}_k + \begin{bmatrix} i_{u_1} \\ i_{u_2} \\ i_{d_1} \\ i_{d_2} \end{bmatrix}_k + aT_s s_b \begin{bmatrix} 3 \\ 6 \\ 3 \\ 6 \end{bmatrix} V_{dc} \quad (11)$$

Similarly, using (10) and (8), the discrete time representation of the subsystem 2 is,

$$\begin{bmatrix} v_a \\ v_b \\ v_c \\ i_a \\ i_b \\ i_c \end{bmatrix}_{k+1} = \begin{bmatrix} 1 & 0 & 0 & f' & 0 & 0 \\ 0 & 1 & 0 & 0 & f' & 0 \\ 0 & 0 & 1 & 0 & 0 & f' \\ g' & 0 & 0 & h' & 0 & 0 \\ 0 & g' & 0 & 0 & h' & 0 \\ 0 & 0 & g' & 0 & 0 & h' \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ i_a \\ i_b \\ i_c \end{bmatrix}_k - f' \begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \\ 0 \\ 0 \\ 0 \end{bmatrix}_k \quad (12)$$

where,

$$f' = -\frac{T_s}{3\,C_f} \qquad g' = \frac{T_s}{L_L} \qquad h' = 1 - e'\,R_L \quad (13)$$

III. Model Predictive Control Strategy

A. Control Overview

Considering that the AMCSI has 81 valid states, the controller must take into account 162 possible combinations due to the 2 states for variable s_b of the current source. Then, the control strategy must calculate the prediction of all the state variables and compute which one of the switches combination minimizes the global cost function (defined in next section). To take into account the delay introduced by the computation, the predictive controller outputs at time k will be applied at the time instant $k + 1$. This imposes the restriction that all the calculations necessary to perform the predictive control must be performed in less than T_s seconds. It is important to highlight that inverter currents in the sampling instant $k + 1$ depends on the switching states at time k, this implies that the load variables $v_{a,b,c}$ and $i_{a,b,c}$ can be predicted only for the $k + 2$ instant. Therefore, a change in the switching states at time k is reflected in the load variables in the $k + 2$ instant, as depicted in [23].

B. Cost Function

In order to complete the predictive algorithm, a global multi-term cost function is defined aimed to include different control objectives. As explained earlier, the cost function must consider each possible combination of switches at time $k + 2$ and the controller will select the state that minimizes the functional.

Given a current reference, $i_{dc_{ref}}$, the individual references for each inverter are generated taking into account the asymmetric distribution of the dc currents, i.e., currents i_{u_1} and i_{d_1} are equal to $\frac{2}{3}i_{dc}$ and i_{u_2} and i_{d_2} are set to $\frac{1}{3}i_{dc}$. Hence, the cost term associated with the current references results,

$$c_{i_{dc1}} = \left(i_{u_{1_{k+2}}} - \frac{2}{3}i_{dc_{ref}}\right)^2 + \left(i_{d_{1_{k+2}}} - \frac{2}{3}i_{dc_{ref}}\right)^2 \quad (14)$$

$$c_{i_{dc2}} = \left(i_{u_{2_{k+2}}} - \frac{1}{3} i_{dc_{ref}}\right)^2 + \left(i_{d_{2_{k+2}}} - \frac{1}{3} i_{dc_{ref}}\right)^2 \quad (15)$$

On the other hand, in order to include the output voltages at the load within the cost function, the sum of the quadratic errors with respect to a voltage reference is proposed,

$$c_{v_{ref}} = (v_{a_{k+2}} - v^*_{a_{k+2}})^2 + (v_{b_{k+2}} - v^*_{b_{k+2}})^2 + (v_{c_{k+2}} - v^*_{c_{k+2}})^2 \quad (16)$$

In this case, voltage references are required for the $k+2$ instant; then, a fourth order Lagrange extrapolation is used, as explained in [23]. In order to reduce the number of commutations, a term that penalizes the number transitions between sampling instants is included. Then, the number of switches that change at each sampling time is

$$N_{sw_\eta} = \sum_{i=1}^{6} \left| s_{i_{\eta_{k+1}}} - s_{i_{\eta_k}} \right| \quad (17)$$

Therefore, the term associated with the commutation of the switches, including the buck converter is,

$$c_{sw} = \lambda_1 N_{sw_1} + \lambda_2 N_{sw_2} + \lambda_{buck} \left| s_{b_{k+1}} - s_{b_k} \right| \quad (18)$$

where the weights λ_1, λ_2 and λ_{buck} are selected to obtain the desired average switching frequency.

Including all the terms presented above, the global cost function is defined as,

$$c_{global} = \lambda_{v_{ref}} c_{v_{ref}} + \lambda_{i_{dc_1}} c_{i_{dc_1}} + \lambda_{i_{dc_2}} c_{i_{dc_2}} + c_{sw} \quad (19)$$

where the weights $\lambda_{v_{ref}}$, $\lambda_{i_{dc_1}}$ and $\lambda_{i_{dc_2}}$ are chosen in order to limit the maximum error of the variables [23].

Finally, the switching state that minimize (19) is selected and applied at instant $k+1$.

IV. Simulation Results

Once the predictive algorithm is programmed, the asymmetric inverter and its control strategy are simulated in the MATLAB/Simulink software. The parameters used are shown in Table II. The following subsections illustrate the performance of the proposed approach under nominal conditions, changes of the output voltage and a step of the input current reference.

A. Nominal conditions

The main waveforms that show the steady state performance of proposed controller are shown in Fig. 2. The output voltage properly tracks its references as shown in Fig. 2 (a) and the resulting line-to-line voltage v_{ab} is presented in Fig. 2 (b). Furthermore, the load current i_a is highly sinusoidal as depicted in Fig. 2 (c); which is achieved with low switching frequency, as shown in Fig. 2 (d). Fig. 2 (e) illustrates that the DC current tracks its reference with a small error, which is a characteristic behaviour of the predictive control with a multifunctional cost function. Fig. 2 (f) shows the asymmetric distribution of currents that follows the 1:2 ratio.

Fig. 3 shows that the i_{inv_a} THD is approximately 20%, while the distortion of i_a is reduced to almost 1% due to the filter capacitors, while the THD of line to line voltage, v_{ab}, is approximately 3%. The performance of the AMCSI is similar to its symmetric counterpart, but using a substantially lesser number of possible combinations [23].

TABLE II
System parameters

Symbol	Definition	Value
V_{dc}	Voltage source	5kV
R_L	Load resistor	15Ω
L_L	Load inductor	6mH
L_{dc}	dc inductor	120mH
L	dc divider inductor base	80mH
C_f	Filter capacitors	22.2μF
T_s	Sampling time	200μs
f_l	Reference frequency	50Hz
$i_{dc_{ref}}$	Reference current	200A
v_{ref}	Reference voltage	2.9kV

B. Output Voltage Step

A step of the reference voltages from 2.9kV to 1.7kV is shown in Fig. 4. The controller tracks with fast dynamic response, as observed in Fig. 4 (a). The corresponding line-to-line voltage v_{ab} is presented in Fig. 2 (b). This reference change implies a reduction in the output current, which reaches its new operating condition smoothly, Fig. 2 (c). The inverter output current is shown in Fig. 2 (d), where it can be observed that only 5 levels are used to track the new reference value.

C. Current Input Step

A negative step of 80A is applied to the DC current reference and the results are illustrated in Fig. 5. Despite the reference change, the output current i_a keeps it expected value, Fig. 5 (a), thanks to the modification of the inverter AC current, Fig. 5 (b). From the AC current waveforms, it is inferable that the AC voltages remain tracking their references. Regarding the dynamic response of the controller, the i_{dc} reaches it new operating point in less than 1 cycle, Fig. 5 (c), and the asymmetric distribution is kept even under the transient condition, as shown in Fig. 5 (d).

V. Conclusion

The presented Asymmetric Multilevel Current Source Inverter provides controlled AC voltage and DC current. It is possible to generate a 7 level current waveform with only two modules, which substantially reduces the number of possible switching combinations compared with its symmetric counterpart, simplifying the evaluation of the predictive algorithm. The proposed controller allows to track the references in steady state as well as during transient conditions, with fast dynamic response. The asymmetric distribution of currents is ensured thanks to the predictive control strategy. The performance of the proposal is similar to the symmetric multilevel inverter in terms of THD and dynamic response, but the main advantage lies in the reduced number of switching devices, which simplifies the predictive control strategy.

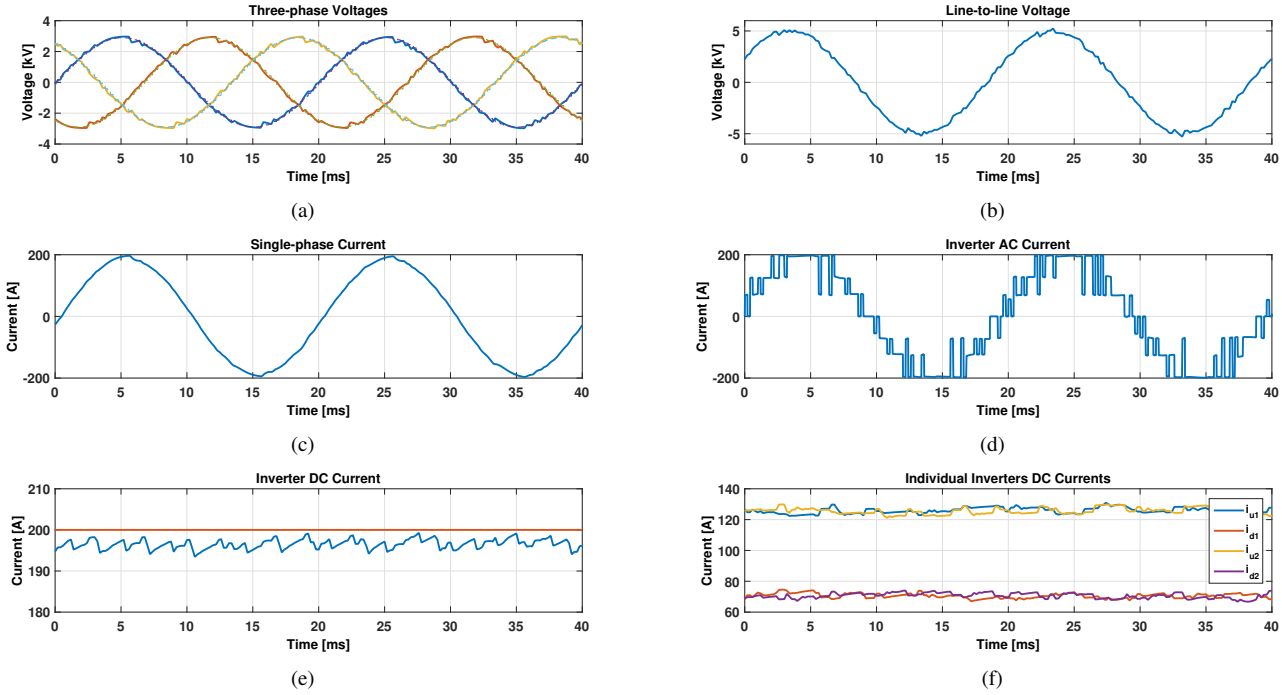

Fig. 2. Simulation results under nominal conditions; (a) phase voltages and references, (b) line-to-line output voltage v_{ab}, (c) output current i_a, (d) inverter output current of phase a, (e) inductor current i_{dc}, (f) inverter asymmetric currents

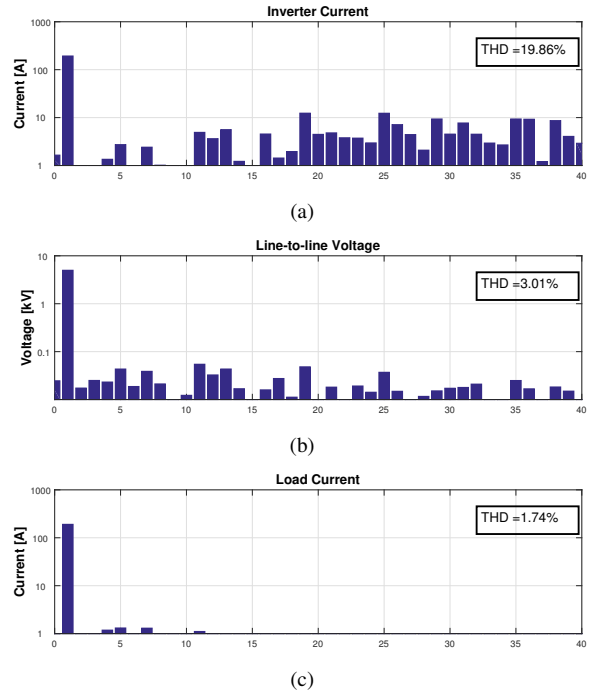

Fig. 3. Waveform spectrum versus harmonic order; (a) inverter output i_{inv_a}, (b) line-to-line output voltage v_{ab}, (c) output current i_a

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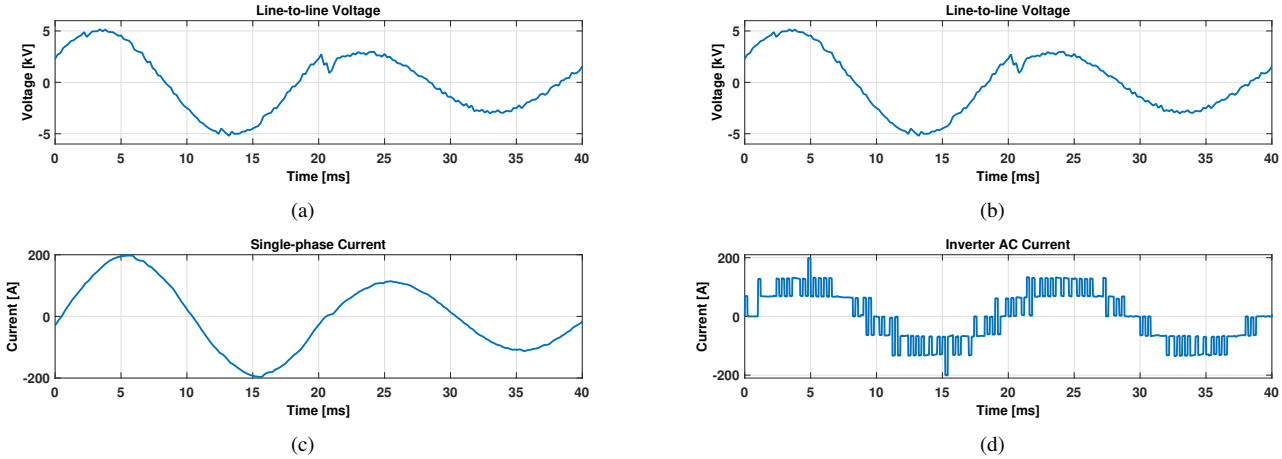

Fig. 4. Simulation results for predictive control of the system with a step change in voltage references; (a) phase voltages and references, (b) line-to-line output voltage v_{ab}, (c) output current i_a, (d) inverter output current of phase a [A]

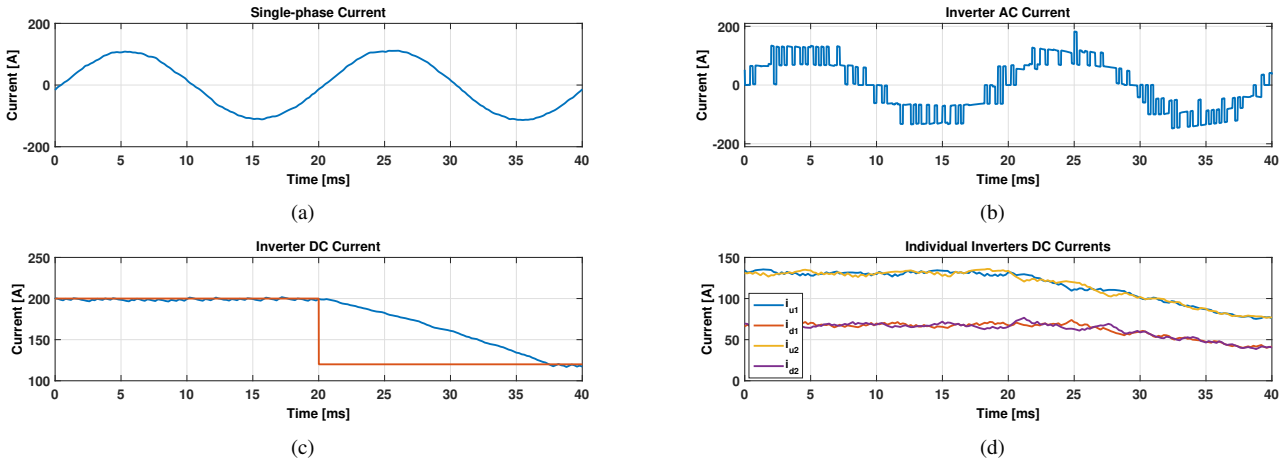

Fig. 5. Simulation results under a step change in current reference; (a) output current i_a, (b) inverter output current of phase a, (c) inductor current i_{dc}, (d) inverter asymmetric currents

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