# Low Noise Front-End and ADC for Real-Time ECG System in CMOS Process

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***Abstract*— This paper presents the design and experimental results of a digital acquisition system based on a chopper-stabilized Instrumentation Amplifier with Common-Mode feedback for CMRR enhancement. Chopping techniques are used to remove both offset and flicker noise, detrimental effects characteristic of pure CMOS processes. A second-order, discrete-time, single-bit Sigma-Delta ADC with CIFB structure is used to convert the signal into the digital domain where it can be processed in real time to diagnose and report urgencies. Measurements on a 0.6µm process have shown that the input CMRR is boosted by 71dB when the feedback is closed through the patient. The input referred integrated noise for the overall system within the ECG band frequencies of 0.1Hz to 400Hz (including the quantization noise) is 4.2µV$_P$, below the recommended maximum detection error of 10.0µV$_P$.**

***Index Terms*— Analog-digital conversion, Biomedical electronics, Biomedical signal processing, Choppers (circuits), ECG, Electrocardiography, Sigma-delta modulation**

## I. Introduction

IN 2016 71% of the overall amount of deaths occurred due to non-communicable diseases. That gives an estimated amount of 41 million of deaths worldwide, from which the principal cause of such deaths were cardiovascular diseases, with 17.9 million of occurrences [1]. Low cost acquisition systems for real-time Electrocardiography (ECG) can be an important tool to detect and report cardiac events.

The ECG signal is composed by several features, which are usually named by P, Q, R, S and T waves as shown in Fig. 1.

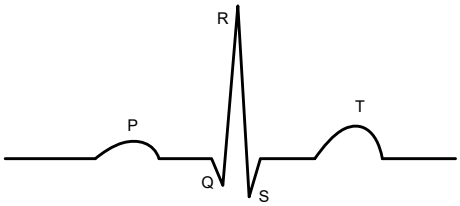


Fig. 1. Simplified representation of a normal sinus rhythm ECG.

In general, the QRS complex has a peak value up to 5 mV. The P wave is in the order of 200 µV [2] but the detection error should be below 10 µV [3]. As a reference, the smallest noticeable feature is usually 25 µV [4].

In terms of bandwidth, the American Heart Association recommends a bandwidth of 150 Hz, but for pediatric studies it must be increased to at least 250 Hz [5]. On the other hand, the low frequency limit is generally set around 0.05 Hz to 0.67 Hz depending on the post-processing technique [5]. In this paper, the system bandwidth will be defined from 0.1 Hz to 400 Hz in order to capture higher frequency content which might be relevant in some applications.

This paper is organized as follows: Section II covers the entire architecture of the system, while design concerns are analyzed in section III. Experimental results are shown in section IV, followed by conclusions in section V. Finally, in section VI, future work is presented.

## II. System Architecture

The proposed system is presented in Fig. 2 and consists of two main stages. The first one is a Front-End subsystem, whose goal is to pre-process the ECG signal by amplifying it and rejecting as much noise and interferences as possible. The second one is a Sigma-Delta Analog-to-Digital Converter (∑Δ ADC).

The Front-End subsystem is composed of a chopper-stabilized Instrumentation Amplifier (IA) and a Common-Mode feedback to improve Common-Mode Rejection Ratio (CMRR). By chopping the amplifier, both offset and flicker noise, a major concern in CMOS processes, are removed. The system achieves superlative low noise levels, comparable with the state-of-the-art implementations [6-8].

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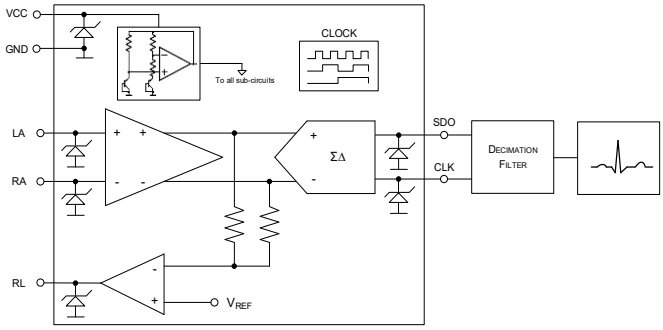


Fig. 2. Simplified block diagram of the complete system.

The ∑Δ ADC, it is a second order, discrete time, single bit implementation with a Cascade of Integrators with a distributed Feedback structure (CIFB).

Finally, there are some other sub-circuits such as a clock generator and a biasing circuit. There are two inputs (Left Arm, Right Arm) and three outputs (Right Leg, the ∑Δ data bit stream and its synchronization clock). Each of these ports has a dedicated Electrostatic Discharge (ESD) protection.

## III. CIRCUIT DESIGN

### A. Front-End Subsystem

Given the limitations of the CMOS-only process available for this application, offset and flicker noise have been a serious concern. A chopper-stabilized topology was employed to modulate these undesired in-band components to higher frequencies where they can be easily filtered away. The implementation of the chopper-stabilized IA is shown in Fig 3.

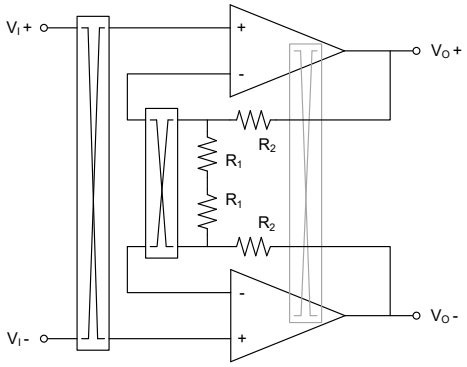


Fig. 3. Schematic representation of the chopper-stabilized IA.

The input signal as well as the feedback are modulated in the voltage domain before entering the IA. However, the demodulation is performed in the current domain before the first transconductance stage. This allows the chopping frequency to be higher than the bandwidth of the amplifier and uses the closed-loop dominant pole as a first order filter for the modulated offset and noise content. The chopping frequency is 100kHz, and the IA bandwidth 30kHz, thus providing a first filtering stage.

On the other hand, one of the main challenges when dealing with ECG signals is to be able to overcome signal wandering (given by, for example, breathing or sudden physical movements). These large in amplitude and low in frequency artifacts are seen as differential signal which can be digitally removed [9,10]. However, the dynamic range of the system has to tolerate such important variations before clipping, therefore the input range of both the Front-End and the ADC have to be set accordingly. That is why the signal path gain has been defined to be 100.

In the same way the system has to cope with such signals, it is crucial to have a high CMRR to attenuate common-mode interferences. In particular, the AC line, whose frequency (50/60 Hz) is within the band of interest. In traditional topologies, this is achieved by an accurate resistor matching. However, in standard CMOS processes this is difficult to achieve unless considering falling back to trimming techniques such as laser trimmed resistors, which have been discarded due to their impact on the overall cost of the product. As a result of this limitation on CMRR, but pursuing its improvement, other techniques such as Faraday shielding [11], adaptive interference canceling techniques [12] and common-mode feedback [13,14] have been considered. This work implements the latter because it does not have the need of any other external components and it prevents the signal to get distorted due to digital filtering in the case of IIR filters or suffered from long transients in FIR filters, which may attempt to the real-time condition.

On account of such approach, the feedback loop is composed by a high gain operational amplifier, the patient, the IA common-mode path and two averaging resistors. The common-mode signal passes over the IA with unity gain and is afterwards compared with a reference input. The consequence of this loop is that any common-mode disturbance on the patient is effectively suppressed before entering the amplifier, adding up directly to the overall CMRR of the system.

### B. Analog-to-Digital Converter

Due to the relatively low frequency content of ECG signals, the inherent anti-alias filter of the IA and the quantization noise shaping properties of ∑Δ converters [15], they are the most suitable for this kind of applications among all other type of converters such as Successive Approximation Register (SAR), parallel conversion (Flash ADC), etc. Therefore, given the discrete nature of the chopper-stabilized Front-End, a discrete time, single bit, ∑Δ structure was implemented to translate the amplified ECG signal to the digital domain. The structure employed was a Cascade of Integrators with distributed Feedback (CIFB) and is shown in Fig 4.

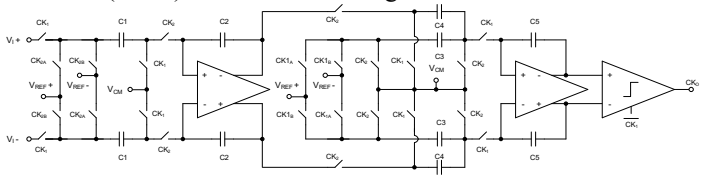

Fig. 4. Schematic representation of the Sigma-Delta Modulator (SDM).

The main requirement for the ADC is to provide a quantization noise that keeps the overall noise below $10\mu V_P$. Thus, an Oversampling Ratio (OSR) of 500 is proposed. This gives a clock frequency of 200kHz which is not as high as to compromise the frequency response of the SDM circuitry.

A second order topology was selected because it requires a lower sampling rate for the same Signal-to-Quantization Noise

Ratio (SQNR) compared to a first order topology. In addition to that, first order SDM tendency for idle-tone generation was an undesired side-effect as well as instability concerns of higher order loops.

The converter reference voltages have been defined as to allow up to a 3V differential input signal. To avoid degradation in the converter performance, input signals should be kept well below this value. For ENOB calculations, dynamic range will be kept to half the differential range.

The 1st stage capacitor sizes were set for SNR = 100 and –3 dBFS input ($C_2/C_1$=3). While the 2nd stage capacitor were set by the minimum allowable capacitance ($C_5/C_3$=9 and $C_5/C_4$=3).

A Cascaded Integrator–Comb (CIC) filter was used to decimate the SDM output. This structure was selected not only because its linear phase response, but also because it is suitable for implementing in silicon (does not require multiplications). In Fig. 5 a block diagram of the CIC filter is shown.

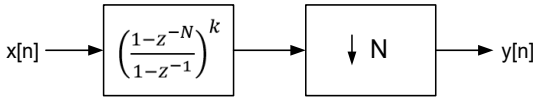


Fig. 5. Block diagram of the CIC filter.

### C. *Auxiliary blocks*

The rest of the complementary blocks composing the system presented in Fig. 1 are the biasing circuitry (Brokaw bandgap reference and current mirrors), a clock generator (Ring oscillator) and several ESD protection circuitry (Grounded-Gate NMOS – GGNMOS). In the case of the voltage reference, substrate PNP are used for the bandgap (single well CMOS process).

## IV. Experimental Results

The whole system has been implemented on a 0.6 µm CMOS process using a Multi-Project Wafer (MPW) service from MOSIS. A silicon microphotograph of the implemented circuit is shown in Fig. 6.

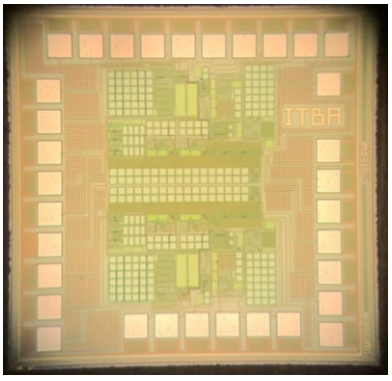

Fig. 6. Silicon die microphotograph.

In previous silicon, the CMRR was boosted by 71dB up to 140dB when the loop was closed through the patient and the input referred integrated noise within the band of interest was 1.17µ$V_{RMS}$ [16].

Fig 7 shows simulations and measurements of the IA Power Spectral Densities (PSD) for previous and actual silicon. Note that the residual flicker noise has been drastically reduced regarding previous silicon while the baseline noise has been kept the same (spot noise: 27nV/$\sqrt{Hz}$ @ 100Hz).

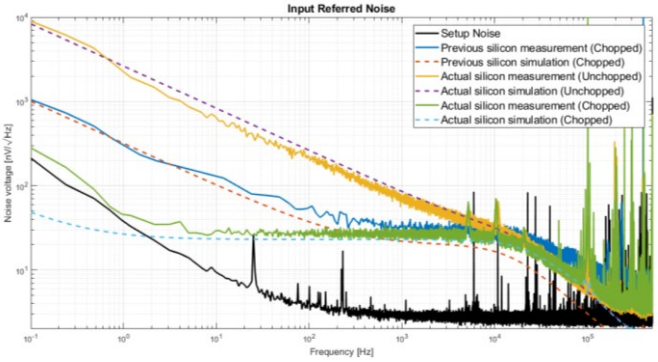


Fig. 7. Comparison of simulated and measured input referred noise PSDs.

The measurements of the integrated RMS noise within the band of interest (0.1 Hz – 400 Hz) for previous silicon was $\sigma_{IA}$ =1.17µ$V_{RMS}$ while for actual is $\sigma_{IA}$ =0.66µ$V_{RMS}$ and the corresponding simulations were predicting 1.00µ$V_{RMS}$ for previous and 0.37µ$V_{RMS}$ for the actual. Such difference in actual measurement can be understood based on the fact that the setup noise (mainly conditioned by the scope probe) has predominant components below 2Hz as shown in Fig. 7 and its integrated noise is 0.27µ$V_{RMS}$.

The converter output spectrum is presented on Fig 8, where the +40 dB/decade noise shaping slope, characteristic of second order ∑Δ converters, is clearly seen. The integrated noise in the band of interest is $\sigma_Q$ =1.18µ$V_{RMS}$ input referred.

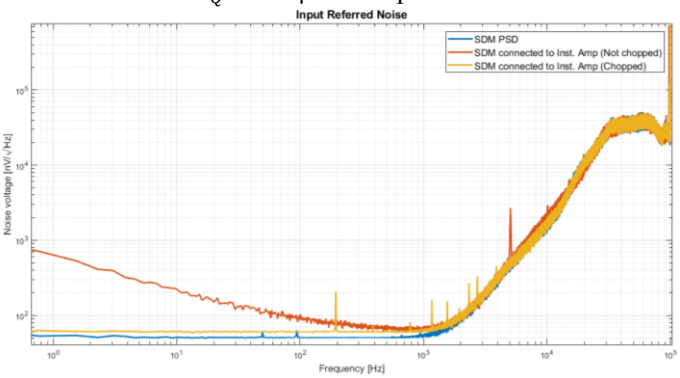


Fig. 8. Measurement of the input referred noise PSD of the SDM.

The total input referred noise considering both the IA and the quantization noise of the ∑Δ gives an overall detection error of 1.42µ$V_{RMS}$ and a 3σ equals to 4.2µV. Spot noise for the ADC alone is 50.8nV/$\sqrt{Hz}$ @ 100Hz and adding the IA it becomes 59.1nV/$\sqrt{Hz}$ @ 100Hz.

The Effective Number of Bits (ENOB) of the ADC is given by (1) and considering the 3σ calculated before, the ENOB for the implemented system is 17.91 bits.

$$ENOB = \log_2(SNR) = \log_2\left(\frac{\sum\Delta\, Range/2}{3\sigma_{IA}+\sqrt{12}\sigma_Q}\right) \qquad (1)$$

The results of the entire system described in section III with a real patient is presented in Fig. 9. Note that typical deflections are identified and even the smallest deflections (P, Q, and S) are clearly identified thanks to the low noise of the system. Moreover, the system bandwidth is high enough to amplify high frequency components (R) without any noticeable distortion on the signal.

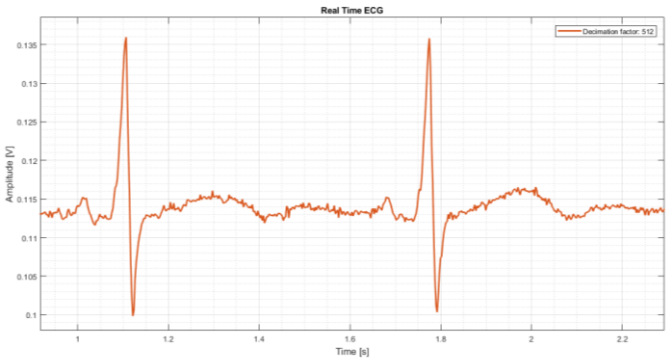

Fig. 9. ECG signal processed in real time.

Noise measurements have been performed using a scope LeCroy 606Zi and a differential active probe LeCroy AP033.

Finally, Table I is included to compare the performance with other state-of-the-art systems.

TABLE I
PERFORMANCE OF ECG SYSTEMS

| | Noise | BW | CMRR | Real Time? | Process |
|---|---|---|---|---|---|
| This work | $1.4\mu V_{RMS}$ $59nV/\sqrt{Hz}$ | 400 Hz | 140dB[a] | Yes | 0.60µm |
| [7] [a] | $1.2\mu V_{RMS}$ [b] | 200Hz | 110dB | Yes | 0.18µm |
| [16] | $90nV/\sqrt{Hz}$ | 100Hz | 72dB | Yes | 0.35µm |

a: Simulated result

b: Low noise amplifier (25.4-25.6kHz)

## V. CONCLUSIONS

A chopper-stabilized Front-End amplifier with common-mode feedback and a second-order, discrete time, single bit, Analog-to-Digital ∑Δ converter for real-time ECG applications was successfully implemented on a 0.6µm CMOS process. The results are showing that the detection error limit of $10\mu V_P$ is successfully achieved by the system, whose overall input referred noise considering both the IA and the ADC is $4.2\mu V_P$.

## VI. FUTURE WORK

Even though the solution proposed is working as expected and is meeting the system specifications, future work should further develop the actual system and provide an on-chip decimation filter as well as digital processing (for example anti-wandering filtering to allow the system to be used as an automated real time ECG for beat classification).

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